Design and Development of Directional Overcurrent Relay for Parallel Feeder Protection-A Lab Prototype

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Abstract:- Directional over-current relay plays a vital role in power system protection. These relays are used in power system protection. Here, an effort is proposed to develop practical panel for power system protection lab. It includes design simulation and implementation of directional over-current relay for parallel feeder protection.

Keywords:- Directional relay, power system, feeder, over-current.

I. INTRODUCTION

The demand of the electric power is increased at a very fast rate. This necessitates the installation of transmission line reaching to all the areas of the state. Also the efficiency of transmission, when large bulk of power is to be transmitted at very long distance should be high. It requires extra high voltage and ultrahigh voltage transmission line to be erected. The voltage of transmission has to be touched the figure 400 KV and still higher voltages of transmission are planned. The idea of national grid needs long ultrahigh voltage transmission line to be installed between different states of the nation. These Transmission line are required to be protected by comprehensive and quite complicated protective relays so that the power interruption is reduced to minimum with regard to the time of interruption and area affected by power interruption. The protective scheme must operate fast and selectively before the power system become unstable. This project is dedicated to protection scheme for parallel feeder using directional over-current relay

II. OVER CURRENT RELAY

The protective relaying which responds to a rise in current flowing through the protected element over a pre-determined value is called over-current protection and the relays used for this purpose are known as over-current relays.

A. Over current relay

Parallel feeder protection can be provided with normal over-current relays, if the minimum Parallel feeder current is sufficient in magnitude. The design of a comprehensive protection scheme in a power system requires the detailed study of time-current characteristics of the various relays used in the scheme. Thus it is necessary to obtain the time current characteristics of these relays supplied by 24V DC. All the measurements are made at 230 V using harmonic analyzer. Harmonic spectrum for each load is plotted showing magnitude of each harmonic frequency that makes up a distorted waveform. The magnitude of each harmonic frequency can be expressed as a percentage of fundamental. Total harmonic distortion is defined from harmonic spectrum as the ratio of the RMS sum of all harmonic frequencies to the RMS value of the fundamental.

Fig. 1 shows constructional schematic of over current relay:

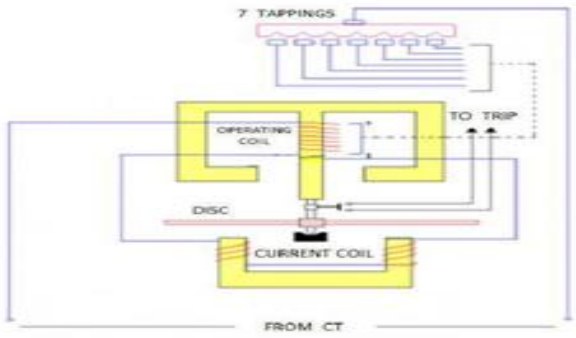

Fig.1: Schematic of over-current relay (OCR)

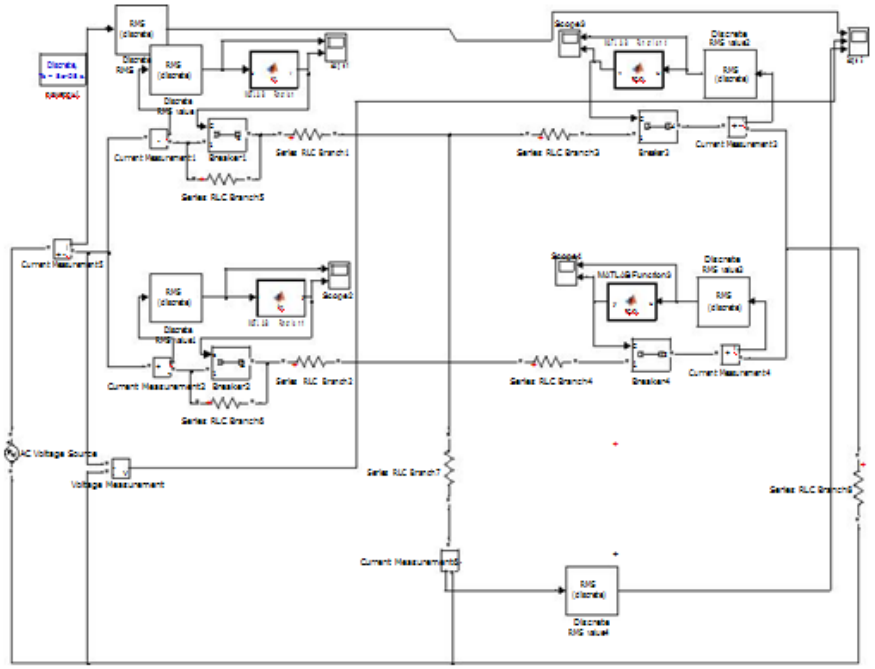

Fig.2: Simulation model of over-current relay (OCR)

Fig. 2 and Fig. 3 showsimulation model of over-current relay and its voltage and current waveforms respectively.

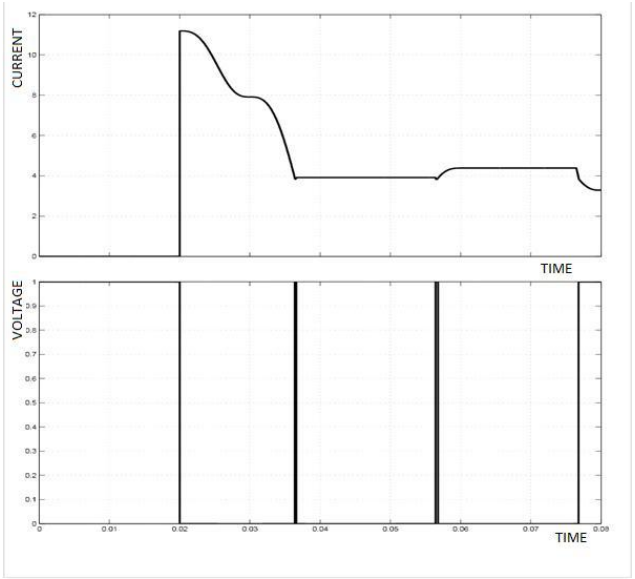

Fig.3: Voltage and current waveforms of over-current relay

B. Directional Over Current Relay

To protect ring or loop networks directional over current relays are commonly employed. The directional Element is added with the over-current relay in order to minimize the outage area. The OCR relay designed above can be modified to behave also as a directional O.C. relay simply by incorporating a directional feature with the relay.

If „Ψ" (let) is the angle between current in a phase and voltage on that phase then -90o<Ψ< 90o shows Normal direction of load flow 90o>Ψ> 270o shows Reversed power flow Fig. shows that during normal conditions (-90o<Ψ< 90o) the overlapping interval between voltage and current is longer than their non-overlapping interval whereas under reversed power flow conditions (90o>Ψ> 270o) the opposite is true.

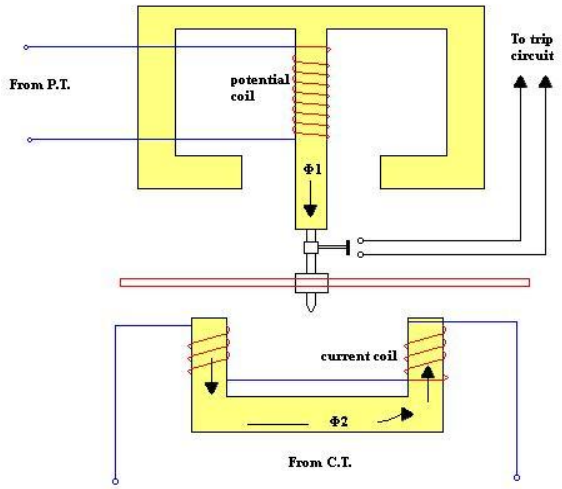

Fig.4: Schematic of directional over-current relay (DOCR)

III. DESIGN OF PARALLEL FEEDER PROTECTION SCHEME

A. Application scheme

Fig. 5 shows parallel feeder protection scheme.

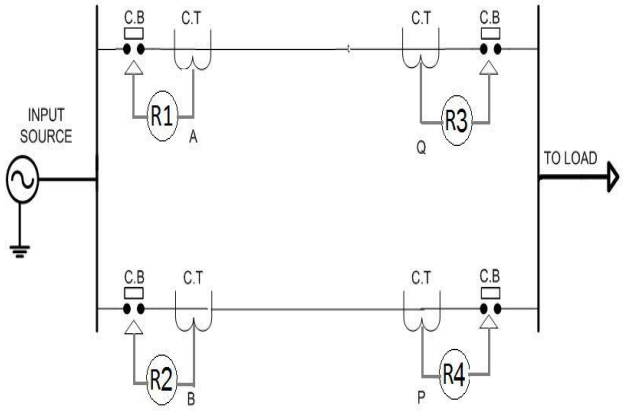

Fig.5: Parallel feeder protection scheme

Referring to above figure, only line AP should trip in case of fault at the point F as shown and not line BQ. After interruption of fault, by tripping line AP due to operation C.B of A & P, full load power has to be transferred along line BQ for a short time during which suitable load shading measures are taken by power engineers.

However if directional feature is not added to relay at Q, the relay at P, Q, B will trip. The operation of relay at B can be delayed but relay at Q cannot be delayed with respect to relay at P because in case of fault in feeder BQ the requirement demands delayed operation of P with respect to Q. Therefore for satisfying the principle of discrimination for selective operation relay at Q & P should be given directional features as shown by arrowheads in the figure above.

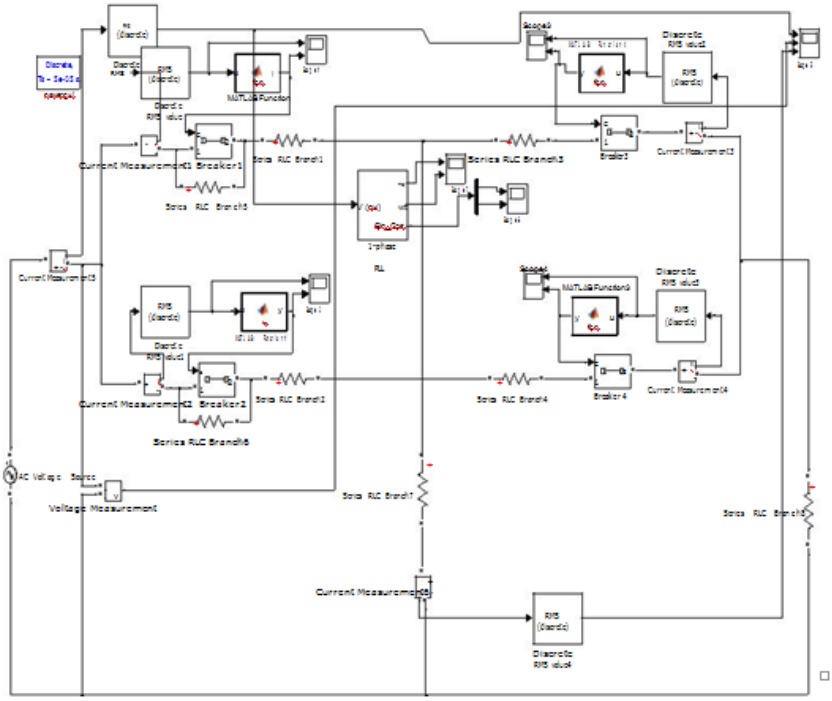

Fig.6: Simulation model of parallel feeder protection scheme with DOCR

B. Relay setting calculations-PSM and TMS

Relay setting calculations for PSM and TMS are shown below: •

$I_{rated} = V/R_{eq} = 230/(9+185) = 1.18A$

- $I_{F1(MAX)} = V/R_{F1} = 230/(9+9) = 12.77$ A
- $I_{f2(max)} = V/R_{f2} = 230/(9+9+9+9) = 6.38$ A
- $I_{fl} = I_{pick\ up} = I_{rated}$ +25%of I_{rated}

=1.18 + (0.25 x 1.18)=1.18+0.295 • $I_{fl}=I_{pick\ up}$=1.475

• PSM of $R_1=I_{fl}/I_{pick}$=12.77/1.475=8.675 • PSM of $R_3=I_{F2}/I_{pick\ up}$=6.38/1.475=4.325 • Time of operating of relay R_3,

$T_{R3} = 0.14 * TMS / (PSM)^{0.02}-1 = 0.14*0.1/(4.325)^{0.02}-1=0.471$ sec.

- Here, $T_{cb},R_3=0.5$ sec is given

So,$T_{cb},R3+T_{R3}=0.5+0.471=0.971$ sec.

- Here, overshoot time of relay $R_2$is of 0.971 sec

So,$T_{os},R2$ =10% of ($T_{cb},R3+TR3$)=0.971*0.1

- $T_{os},R2=0.0971$ sec

So, operation time of relay R_2 is,

$T_{R2}=T_{R3}+T_{cb},R_3+T_{os},R2=0.971+0.0971$ $T_{R2}=1.0681$ sec

- The time of operation of relay R_2 can be also

given, $T_{R2}=0.14*TMS/(PSM)^{0.02}-1$

$1.0681=0.14*TMS/(8.657)^{0.02}-1$ $1.0681[(8.657)^{0.02}-1]=0.14*TMS$

TMS=1.0681*0.0441/0.14

TMS = 0.336.

Various relay settings are tabulated in Table I shown below:

Table I: Harmonic distortion due to bridge rectifier at PCC

Sr. No.	Relay	PSM	TSM	TIME OF OPERATION
1	R1	8.657	0.336	1.0681
2	R2	8.657	0.336	1.0681
3	R3	4.325	0.1	0.471
4	R4	4.325	0.1	0.471

IV. IMPLMENTATION OF PARALLEL FEEDER PROTECTION SCHEME

Implementation procedural steps are as follows:

A. Power Supply Circuit

- Brief description of operation: Gives out well regulated +5V output, output current capability of 500 mA.
- Circuit protection: Built-in overheating protection shuts down output when regulator IC gets too hot.
- Circuit complexity: Very simple and easy to build.
- Circuit performance: Very stable +5V output voltage, reliable operation.
- Availability of components: Easy to get, uses only very common basic components.
- Applications: Part of electronics devices, small laboratory power supply.

B. Circuit parameters

- 100 KVA, 230/9-0-9, 1-ϕ, Step down Transformer
- IC 7805 & IC 7905
- D1, D2, D3, D4 = Diode
- C1 & C2 = 2200 μF at 25 V voltage rating
- C3 & C4 = 100 μF at 25 V voltage rating
- C5 & C6 = 0.1 μF at 25 V voltage rating

Power supply circuit diagram and implementation of the same has been shown in Fig. 7 and Fig. 8 respectively.

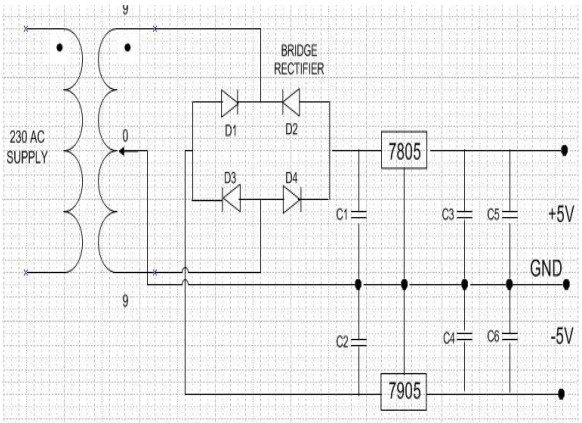

Fig.7: Power supply circuit diagram

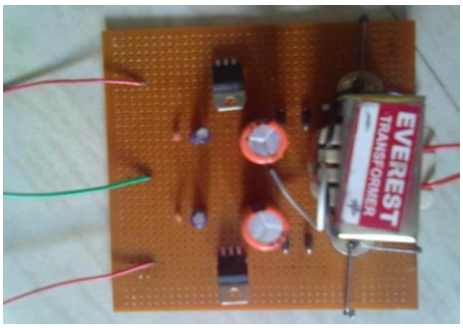

Fig.8: Power supply circuit implementation

C. Current transformer (CT) characteristics

Fig. 9 shows test circuit diagram to obtain CT characteristics.

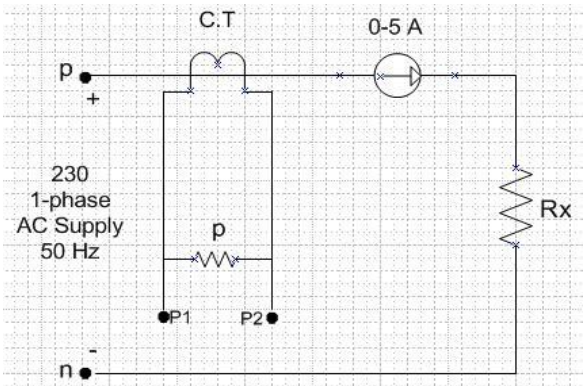

Fig.9: Test circuit diagram to obtain CT characteristics

In parallel with the C.T, if the burden is very less than the current in the C.T will cross the limit. And, if the burden is very high value than the current in the C.T cannot reach to the operating value. So, we have to find the linear operating range of the C.T. That can be done by the circuit arrangement as follows:

Table I: Improvement in load current THD

SR NO.	I(A) (Current in secondary of C.T.)	V(mV) (Voltage across C.T. burden)
1	0.5	1
2	1.5	2
3	2.5	3
4	3.5	4
5	4.5	5
6	5.5	6.5
7	6.2	8

Corresponding CT output waveform is shown in Fig. 10.

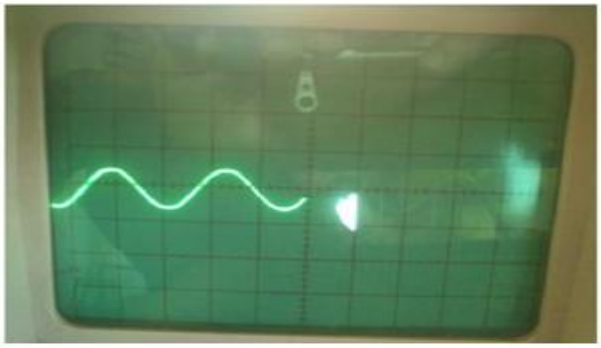

Fig.10: CT output waveform

The open-loop non-inverting amplifier. In this configuration the input is applied to the non-inverting input terminal, and the inverting terminal is connected to ground.

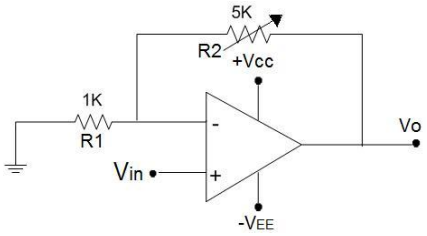

Fig.11: Circuit diagram of non-inverting amplifier

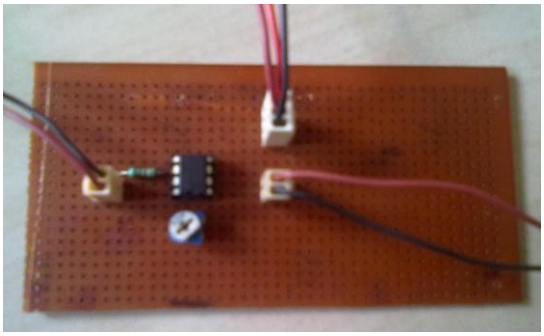

Fig.12: Implementation of of non-inverting amplifier

Fig. 11 & Fig. 12 show non-inverting amplifier circuit diagram and implementation of the same respectively.

D. Summing amplifier

If input voltage source and resistors are connected to the non-inverting terminal. The circuit can be used either as a summing or averaging amplifier through selection of appropriate values of resistors. Using the superposition theorem, the voltage V_1 at the non-inverting terminal.

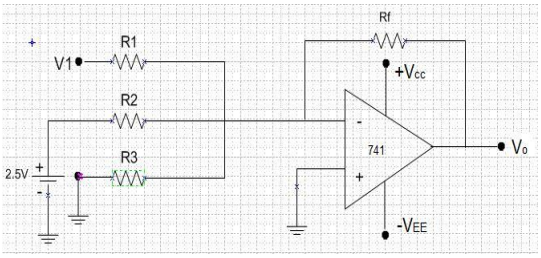

Fig.13: Circuit diagram of summing amplifier

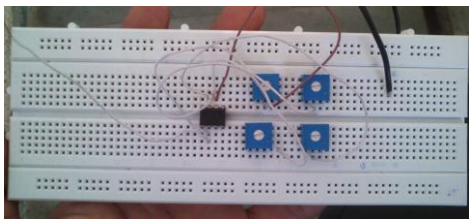

Fig.14: Implementation of summing aplifier

Fig. 13 and Fig. 14 show circuit diagram and implementation of summing circuit.

E. Interfacing 8051 Micro-controller card

Interfacing Micro-Controller card with 8051 (AT89S52) microcontroller Micro-Controller card is preferred due to its small size, high memory capacity ,non-volatile memory, low power consumption and low cost. So this memory product is used in most of the consumer electronic products.

If we want a data acquisition system which should store a vast amount of data then Micro-Controller card is very good choice.

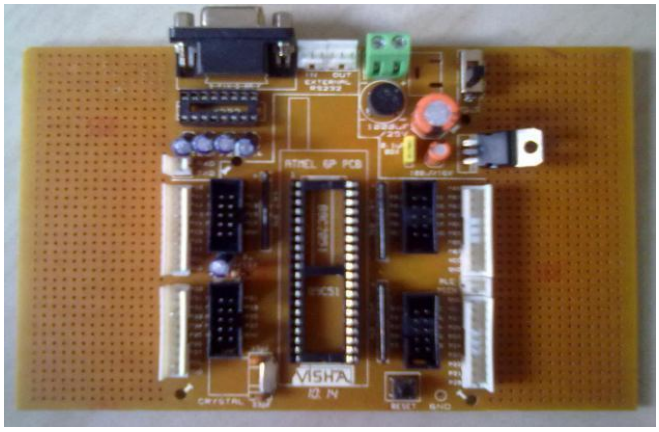

Fig.15: Implementation of 8051micro-controller card

Fig. 15 shows describes the interfacing of the Micro-Controller card with AT89S52 microcontroller.

F. Micro-Controller Programming

The interfacing program is the most basic part of the numerical relay. That part can sense the current and voltage value at a particular time instant. It process the input data and give the command to the offset part of the numerical relay.

After sensing the data it verify the input data with reference to the predefine command. If the condition is satisfy than it passes the trip command to the offset part otherwise it continuing to sense the data. Micro-Controller card works at 5v CMOS level. The detailed programming is given in Appendix.

V. CONCLUSIONS

Design and manufacturing of prototype directional overcurrent relay by the local manufacturers is produced as an alternative solution for power system protection. The paper presents low cost, high performance overcurrent relay that is used in parallel feeder protection. Moreever, the same relay can be used for several protection applications like, overcurrent, earth fault, restricted earth fault, etc.

The designed hardware platform can be used also for over/under voltage and load shedding protection with simple modification.

VI. APPENDIX

The interfacing programming:

```
#include<reg51.h>
sbit ALE=P1^0;
sbit OE=P1^4;
sbit
EOC=P1^5;
sbit SC=P1^6;
sbit A=P1^1;
sbit  b=P1^2;
sbit C=P1^3;
sbit x=P2^0;
sfr mydata=0x80;

void main()
{
mydata=0xff;          // P0 get use as input.
TMOD = 0x20;          // TMOD: timer 1, mode 2, 8-bit reload
TH1= 0xFD;            // TH1: reload value for 9600 baud @ 11.0592MHz
IE = 0x88;            // Interrupt flag IE=10001000=88H
SCON  = 0x50;         // SCON: mode 1, 8-bit UART, enable rcvr
```

```
PCON=PCON&0x7F;
C=0;
b=0;
A=1;
ALE=0;
SC=0;
OE=0;
EOC=1;
TR1 = 1;            // TR1:  timer 1 run
While (1);
}

void timer1 (void) interrupt 3
{
int i=0;
unsigned char m=0; ALE=1;
for (i=0;i<=10;i++)
{}
SC=1;
for (i=0;i<=10;i++)
{}
ALE=0;
SC=0;
while     (EOC==1);
while     (EOC==0);
OE=1;
for (i=0;i<=100;i++)
{}
m= mydata;
for (i=0;i<=100;i++)
{} SBUF=
m;
while (TI==0);
TI=0;
}
```

Define variable in REG51:

```
#ifndef __REG51_H
#define __REG51_H

sfr P0 = 0x80; sfr
P1 = 0x90; sfr P2
= 0xA0; sfr P3 =
0xB0; sfr PSW =
0xD0; sfr ACC =
0xE0;
sfr B = 0xF0; sfr
SP = 0x81; sfr
DPL = 0x82; sfr
DPH = 0x83; sfr
PCON = 0x87; sfr
TCON = 0x88;
sfr TMOD = 0x89;
sfr TL0 = 0x8A;
sfr TL1 = 0x8B;
sfr TH0 = 0x8C;
sfr TH1 = 0x8D;
sfr IE = 0xA8; sfr
```

```
IP = 0xB8; sfr
SCON = 0x98; sfr
SBUF = 0x99;

/* BIT Register */
/* PSW */
sbit CY = 0xD7;
sbit AC = 0xD6;
sbit F0 = 0xD5;
sbit RS1 = 0xD4;
sbit RS0 = 0xD3;
sbit OV = 0xD2;
sbit P = 0xD0;

/* TCON */ sbit
TF1 = 0x8F;
sbit TR1 = 0x8E;
sbit TF0 = 0x8D;
sbit TR0 = 0x8C;
sbit IE1 = 0x8B;
sbit IT1 = 0x8A;
sbit IE0 = 0x89;
sbit IT0 = 0x88;

/* IE  */
sbit  EA  =  0xAF;
sbit  ES  =  0xAC;
sbit ET1 = 0xAB;
sbit EX1 = 0xAA;
sbit  ET0  =  0xA9;
sbit EX0 = 0xA8;

/* IP  */
sbit  PS  =  0xBC;
sbit PT1 = 0xBB;
sbit PX1 = 0xBA;
sbit  PT0  =  0xB9;
sbit PX0 = 0xB8;

/* P3  */
sbit RD = 0xB7;
sbit WR = 0xB6;
sbit T1 = 0xB5;
sbit T0 = 0xB4;
sbit INT1 = 0xB3;
sbit INT0 = 0xB2;
sbit TXD = 0xB1;
```

```
sbit RXD  = 0xB0;

/* SCON  */
sbit SM0 = 0x9F;
sbit SM1 = 0x9E;
sbit SM2 =
0x9D; sbit REN
= 0x9C; sbit TB8
= 0x9B; sbit RB8
= 0x9A; sbit TI =
0x99; sbit RI =
0x98;
#endif
```

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