Analysis of Low Power and Area efficient CMOS Comparator Design

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Abstract:- In this Paper presents a new dynamic comparator is compared in terms of their voltage, speed and power. A new dynamic comparator which shows lower input offset voltage and high load drivability than the conventional dynamic comparators. This comparator not only achieves low offset but also exhibit high speed and low power in its operation, which can be used for low power high speed ADC application.

Keywords:- ADC,CMOS(Complementary metal oxide semiconductor), low offset, low power, high speed, Conventional dynamic double tail Comparator, Proposed dynamic comparator

I. INTRODUCTION

In The Recent Communication System The Bandwidth Is One Of The Most Important Resources Of The Communication System. Also There Is An Upgrading Demand For The High Data Rate. But As There Is Limited Frequency Resource Available We Need To Limit The Bandwidth. Transmitting The Information Through A Band Limited Channel Whose Signal Bandwidth Is Nearby To The Channel Bandwidth Would Result Into Inter Symbol Interference Which Can Be Problematic At

The Time Of Reception At The Receiver End If It Is Left Uncontrolled [3].

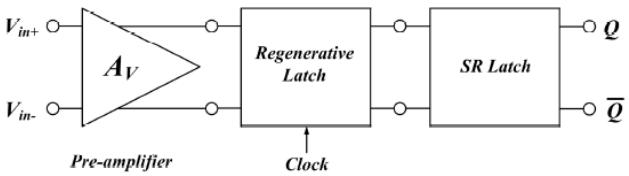


FIG.1 TYPICAL BLOCK DIAGRAM OF A HIGH-SPEED COMPARATOR

This Paper Is Organized As Follows. Section 2 Investigates The Operation Of The Conventional Comparators Of Each Structure Is Discussed. Section 3 Is Discussed Dynamic Comparator Which Is Based On The Structure Section & Simulation Results Are Addressed Followed By Conclusion In Section 4.Simulation Results From Ltspice Using 180nm Technology [1] With Vdd = 0.8v And Their Comparison Is Presented In This Section 4.

II. CONVENTIONAL SINGLE-TAIL COMPARATOR

Comparator Is One Of The Fundamental Building Blocks In Adc. Designing High-Speed Comparator Is More Challenging When The Supply Voltage Is Smaller. In Other Words To Achieve High-Speed, Larger Transistors Are Required To Compensate The Reduction Of Supply Voltage, Which Also Means That More Area And Power Is Low. Developing A New Circuit Structures Which Avoids Too Many Transistors Between The Supply Voltage For Low Power Operation, Especially If They Do Not Increase Circuit Complexity.

Operation :

Conventional single tail comparator have found wide applications in many high-speed ADCs. Since, they can make fast decisions due to positive feedback in the latch. Recently, many comprehensive analysis have been presented, which investigate the performance of these comparators from different aspects, such as noise, offset [2],[3].

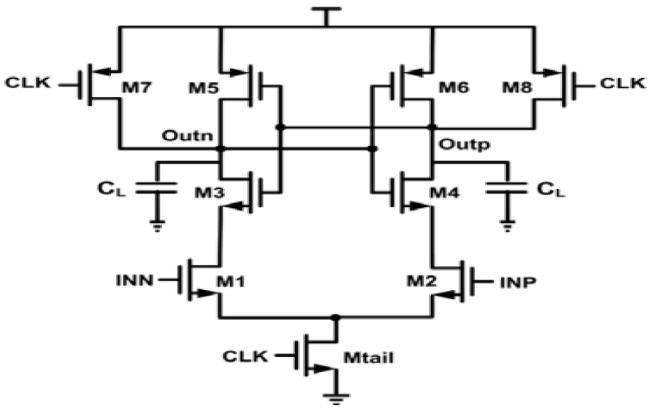


Fig.2 Schematic diagram of Single tail comparator

(2) Conventional Double-tail Comprator :

A Conventional double-tail comparator is shown in figure (3).This Comparator can operate at lower supply voltages compared to the conventional dynamic comparator. The double-tail make possible both a large current in the latching stage and Mtail2, for fast latching free of the input common-mode voltage (Vcm), and a small current in the input stage(small Mtail1), for low offset. The operation of this comparator is as follows fig(3). During reset phase when clk=0, Mtail1 & Mtail2 are off, transistor M3-M4 are pre-charge fn & fp nodes to VDD, which transistors MR1 and MR2 to discharge the output nodes to ground. Then next is decision making phase clk=VDD, then Mtail1 & Mtail2 turn on. After that M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by Itail1/C fn(p) and on top of this , input differential voltage(V) fn(p) will make up.

(3) Double-tail Dynamic Comparator:

A Dynamic double-tail comparator is shown in fig (3). Double tail comparator has two tail transistors. Double tail comparator is used for low power application. In this technique, increase the voltage difference between the output nodes in order to increase the latch regeneration speed. For this purpose, two control transistors have been added to the first stage in parallel to m3 and m4 transistor but in a cross coupled manner. Double tail comparator has two operation nodes, the reset phase and the decision making phase. When clk=0 known as reset and clk=VDD, it is known as decision making phase. When clk=0, nMOS transistor is in off and pMOS transistor is in on. When clk=VDD nMOS is in om and pMOS transistor is in off.

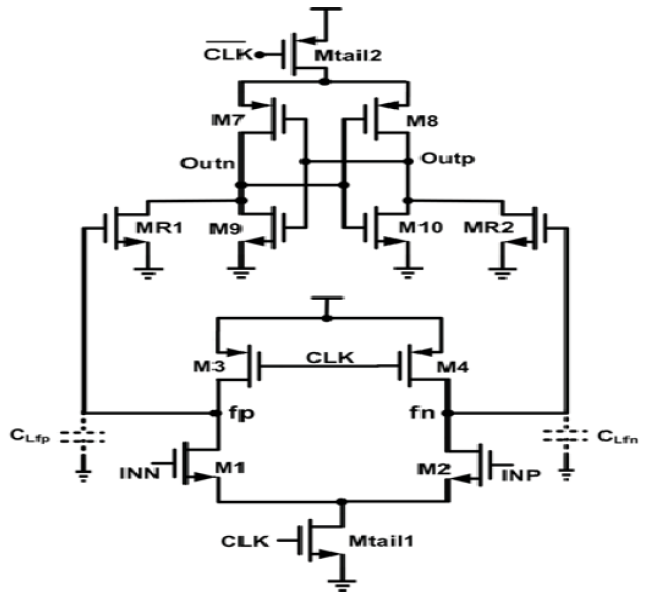


Fig.3 Conventional Double-tail Dynamic Comparator

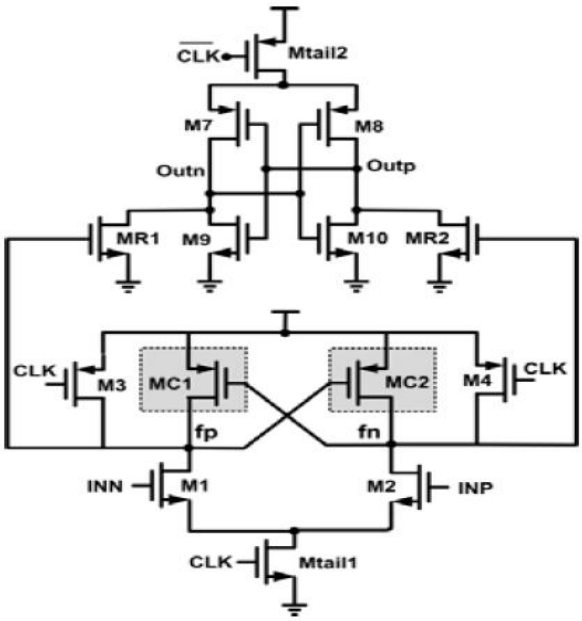
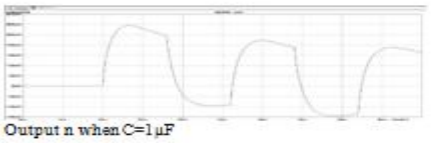


Fig.4 Dynamic Dual-tail Comparator

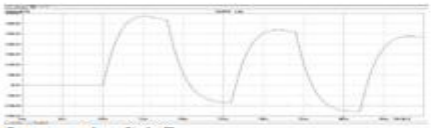
III. SIMULATION RESULT

Conventional Single-tail Comparator :

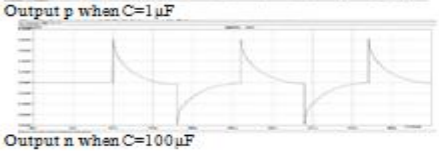
Clk input signal



Output n when C=1 µF

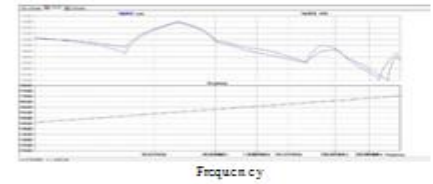


Output p when C=1 µF

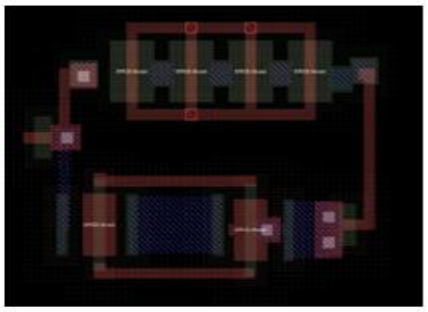


Output n when C=100 µF

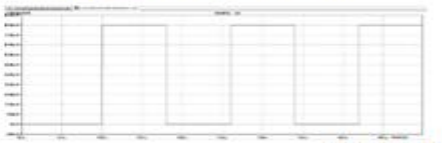
Output p when C=100 µF



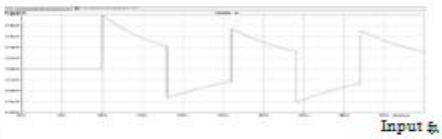
Frequency



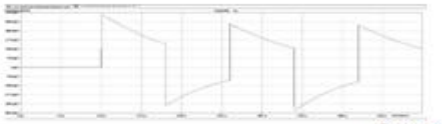
(2) conventional dual-tail comparator analysis :



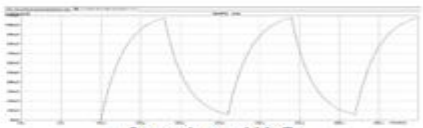
Clk input signal



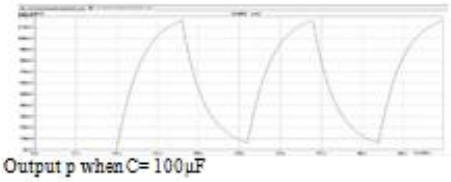
Input



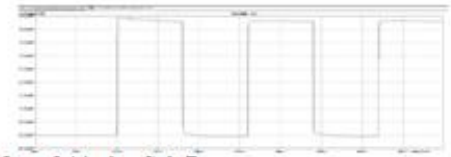
Input



Out n when c= 100 µF

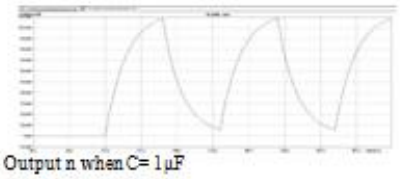


Output p when C= 100 µF

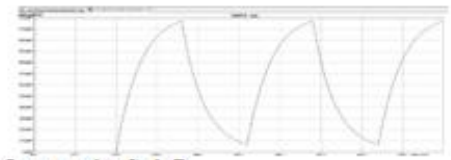


Input fn(n) when C=1 µF

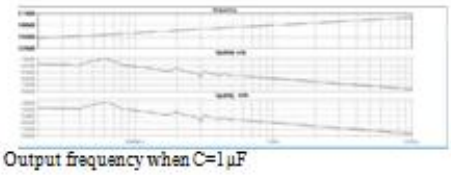
Input fp(p) when C=1 µF



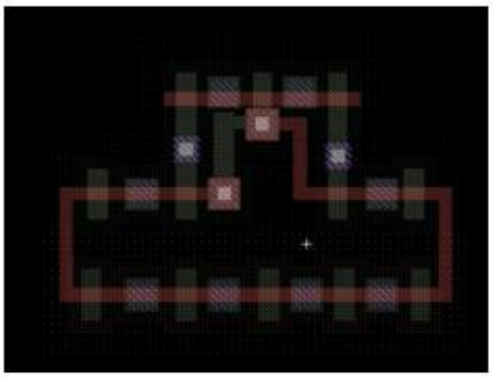
Output n when C= 1 µF



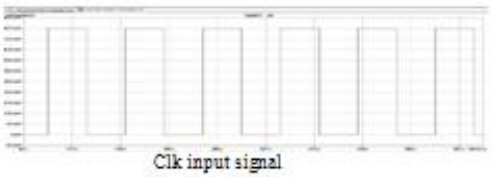
Output p when C= 1 µF



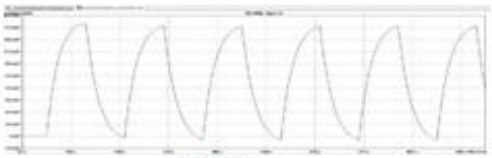
Output frequency when C=1 µF



(3) Dynamic Dual-tail comparator

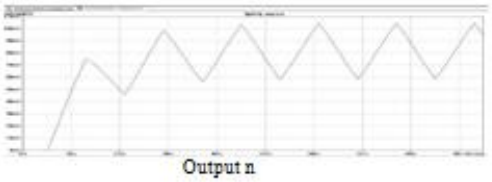


Clk input signal

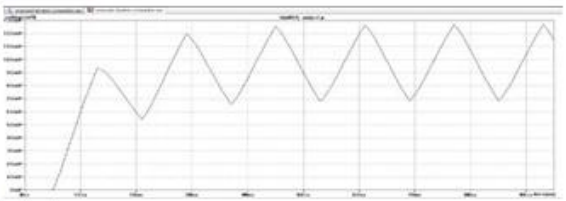


Input fn

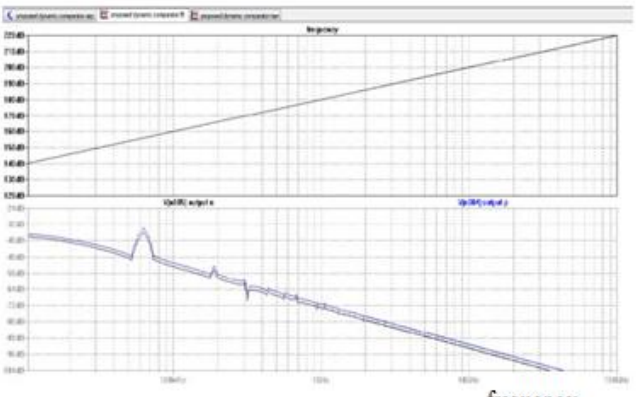
Input fp



Output n



Output p



frequency

Table.1 Number of Transistor on each Comparator

Circuit	**No. of Transistor**
Conventional single-tail Comparator	9
Conventional double-tail Comparator	12
Dynamic Dual-tail Comparator	14

IV. CONCLUSION

In this paper present a various circuit we present a double tail dynamic comparator with more no of transistor .This new dynamic double-tail comparator will reduce voltage, delay, power and high speed compare to other comparator.

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