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Design an H-Encoder/Decoder with Adaptive Logic

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Abstract:- In this paper, we perform a high-performance H-encoder/decoder with adaptive logic architecture for the VLSI implementation. By executing the coupling switching activity (C.S.A) obtained by different data encoding techniques (D.E.T). The proposed system called as Adaptive Efficient Encoding technique (A.E.E.T) is introduced. The proposed encoding is inversion operation which is restricted to some encoding schemes. As the adaptive effective encoding technique gives better delay. The Xilinx 13.1 software is used for execution with Family SPARTAN 3E. The device and package used are XC3S100E and VQ100. Preferred verilog language to execute H-encoder/decoder with adaptive logic

Key terms: A.E.E.T, C.S.A, D.E.T, Encoder, Decoder

I. INTRODUCTION

Encoder is a digital circuit that performs the inverse operation of decoder it has 2^n input lines and n output lines and it generates the binary code corresponding to the input values. Encoders are of two types they are incremental encoder (rotary/shaft encoder) and absolute encoder. Shafting encoder is an electro mechanical device which helps to convert the angular position or motion of a shaft or axle to an analog code or digital code. It is a pulse generator that provides a square wave signals and a zero index[7]. To overcome this problem we gone through absolute encoder it has been developed to compensate for the performance and limitations of shaft

It is a pulse generator that provides a square wave signals and a zero index. To overcome this problem we gone through absolute encoder it has been developed to compensate for the performance and limitations of shaft encoder this encoder must be reserved after a power interruption zero reset is help to obtain the mechanism angular position and sensitivity of interference[1]. This absolute encoder supplies the shaft position as a binary code. The output code is unique for each position

In this paper we focused on techniques aimed at adaptive encoding technique of power consumption by the Xilinx software here we use encoder and as well as decoder with the help of adders[4]. The proposed encoding schemes which are transparent with respect to the pulses implementation are presented and discussed at both binary/algorithmic level and the architectural level by means of simulation on synthesis and real traffic scenarios this result shows that by using the proposed encoding scheme up to 52% of power and 16% of energy can be saved without any significant degradation.

II. EXISTING STAGE

SCHEME 1: To exist encoding technique I use encoder and decoder in scheme I focus on reducing the number of TYPE 1 and TYPE 2 transistors[1]. The scheme 1 compares the present data with previous one (flit) to decide whether the given input is odd inversion or no inversion of the present data can lead to power reduction if the previous bit is odd inverter before being transmitted, the dynamic power on the links are the self transition activity of Types I, II, III and IV, respectively. For each transition the relationship between the coupling transition activities of the flit when transmitted as its bits are odd inverted.

Here if the flit is odd inverted, Types II, III and IV transitions convert to the type I transitions. In case of transition types the type I transitions, the inversion of one of the Type II, III or Type IV transition respectively[1]

SCHEME 2: Here I make use of both odd and full inversion the full inversion operation converts Type II to Type IV transition. It compares the current data with the flit to decide whether the odd, full, or no inversion of the current data can give rise to the power reduction

The power is dissipated when the flit is transmitted with no inversion, odd inversion and full inversion, respectively. The odd inversion lead to power reduction and the full inversion satisfied inequality. The operating principles of this encoder are similar to the previous encoder. Here again the previously encoded body flit is indicated with inv which defines if it was odd or full inverted (inv=1) or left as it was (inv=0).

SCHEME III: The reason is that the odd inversion converts some of the Type I transition to Type II transition. If the flit is even inverted the transitions are converted to Type IV or Type III transitions. Therefore,

the even inversion may reduce the power dissipation as well. The scheme compares the current data with the previous flit to decide whether it is odd, even, full or no inversion of the current data can give rise to the power reduction[1]. When the flit is transmitted with no, odd, full and even inversion respectively.

III. PROPOSED SYSTEM

H-Encoder

It is better codes of error controlling performance. H-Encoder outputs are not only associated with the encode elements at present, but also affected by several ones before. Data 1 and data 2 are used for describing codes, where data 1 are the input encode elements, data out is the output encode elements and data 2 is the shift register number of encoder

Data 1 and Data 2 are the inputs of the Encoder. Their architecture design with chip registers perform their operations and gives output of the encoder is Data out as shown in fig 1.

H-Decoder

Two parallel binary bits are inputted into the H-decoder with every clock pulse, and then it begins to work when the input enabling signal is valid. Each group consists of two because each current state can be reached by decoder path.

Here Data out is the output of the encoder similarly Data out and Data 2' are the inputs of Decoder. These inputs will perform as per their chip architecture design and the output of the decoder is Data as shown in fig-1.

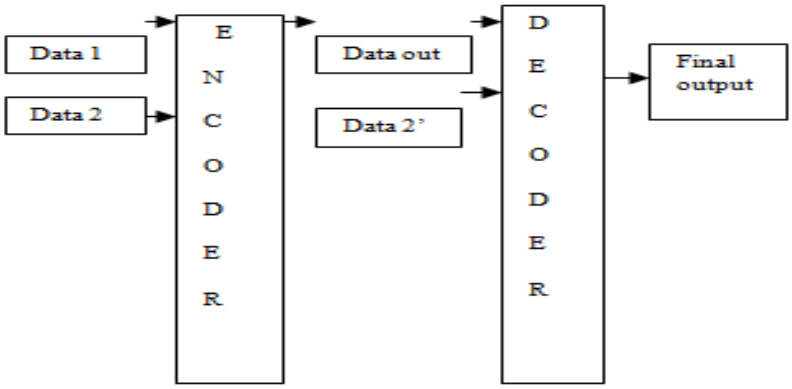

Fig-1 H-Encoder/Decoder with Adaptive Logic

Figure 1 indicates the block diagram of H-encoder/decoder with adaptive logic. The H-encoder/decoder with adaptive logic consists of four shift registers and two exclusive-or gates. Every shift register is equivalent to a flip flop. These four flip flops are connected in series to complete shifting and updating operation under the action of the clock pulse. The exclusive-or gates are used for inner operation of coding data. With every clock pulse the encoder outputs two bits according to the generator polynomials whenever one binary bit is inputted. The output is not only relevant with the current input binary bit, but also influenced by the previous bit for decoder

TECHNICAL SCHEMATIC:

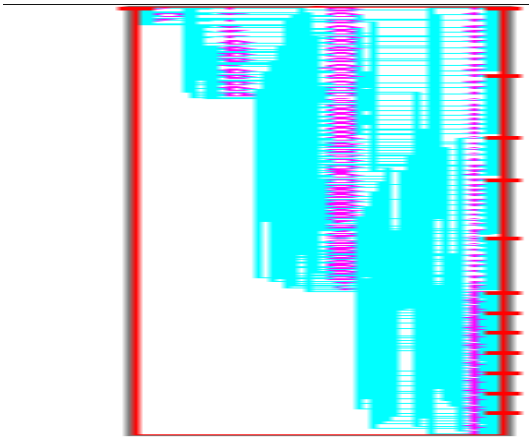

FIG-2 Technical Schematic

Fig-2shows the technical schematic of data adaptive effective encoding techniques

For reducing energy consumption

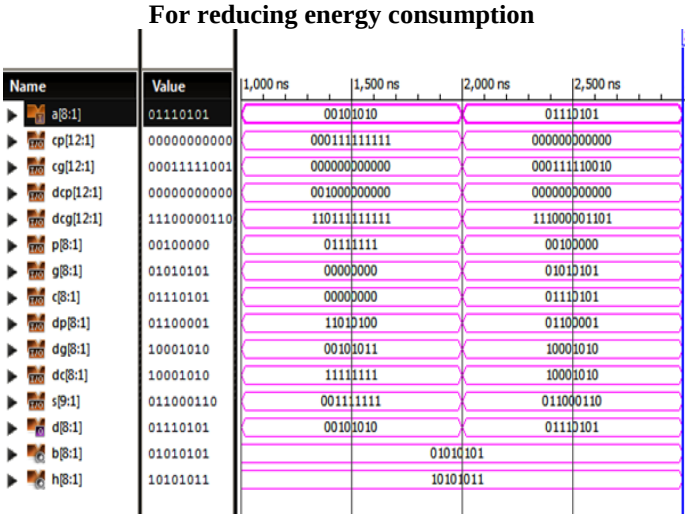

FIG-3 Output Waveforms

IV. OUTPUT WAVEFORMS

Fig-3 shows the output waveforms of data adaptive encoding techniques. Here we have given a[8:1] as a input data for encoder and s[9:1] taken as output for encoder. As well as s[9:1] taken as input data for decoder where as d[8:1] is the output for decoder.

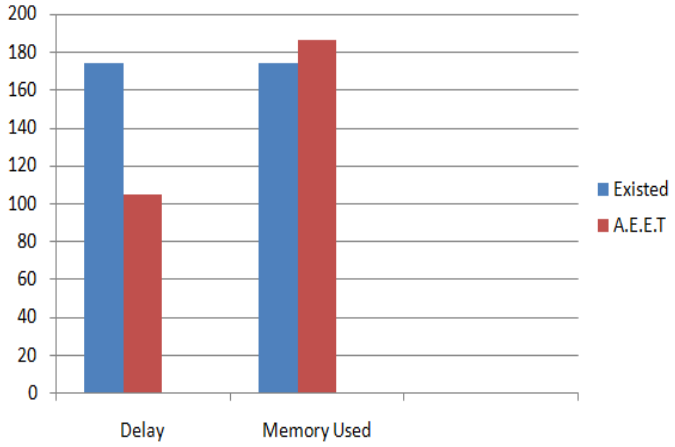

Fig. 4 comparison graph

The table-1 shows the comparison of area and delay for existed technique and proposed technique.

TABLE-1

Technique/parameter	Delay(NS)	Area(MB)
Existed encoding technique	17.38	174
A.E.E.T(proposed)	10.46	186

The H-Encoder/Decoder with Adaptive logic decides the proposed algorithm to work with adaptive logic. The registers are work with the adaptive techniques, by using this technique, the proposed algorithm increases the speed i.e. decrease the delay.

V. CONCLUSION

A.E.E.T is based on the proposition that Genetic algorithm finds good solutions to a problem. Studying the existing encoding schemes I, II & III is proposed. The A.E.E.S encoding scheme. The proposed encoding supports one point crossover as in binary encoding and A.E.E.T crossover as in encoding. The proposed encoding is inversion operation which is restricted to some encoding schemes. A.E.E.T is very efficient in speed. As the adaptive effective encoding technique gives better delay. By using proposed system we can reduce delay by 17.38ns to 10.46ns

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