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Digitally Programmable Grounded Impedance Multiplier

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Abstract:- A novel digitally programmable generalized impedance multiplier is presented. It uses second generation current conveyor and a digital control module. The new multiplier can provide digital control to grounded impedance functions such as, resistor, capacitor, inductor without quantizing the signal. The technique used is simple, versatile as well as compatible for microminiaturization in contemporary IC technologies. The simulation results on digitally programmable generalized impedance multiplier verify the theory.

Keywords:- Current conveyor, multiplier.

I. INTRODUCTION

In recent years the second generation current conveyors (CCIIs) have proved to be functionally flexible and versatile building block. It possess higher signal bandwidth, greater linearity and large dynamic range [1-2]. As a result it is gaining wide acceptance as a building block for designing voltage/current mode analog signal processing circuits [3-6]. In the mixed signal systems the on chip control of the systems' parameter can be provided through digital means with high resolution capability and the reconfigurability[4-7]. However, not much content is available in the technical literature on the subject.

In this paper a novel digitally programmable grounded multiplier (DPGIM) using second generation current conveyor is presented. To demonstrate the versatility of the DPGIM, digitally controlled grounded resistor(R), capacitor(C) and inductor are realized. The circuit consists of a CCII, a digital control module (DCM), which is realized using R-2R ladder and a n-bit switching array, along with impedance under control. The realized DPGIM is simulated for positive and negative resistors using PSPICE.

II. DIGITAL CONTROL MODULE

The realization of the digital control module (DCM) used in the DPGIM is shown in Figure 1(a), which uses R-2R ladder and analog switching array [6]. Its routine analysis yields the output voltage V_2 as

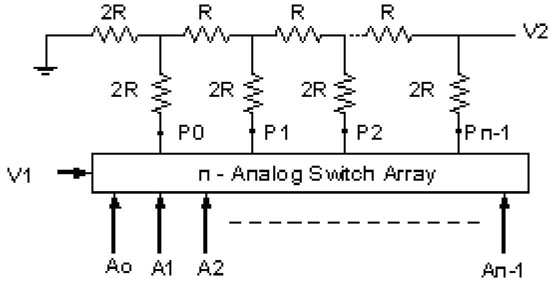

Fig. 1(a): Digital Control Module-The DCM.

$$V_2 = \frac{V_1}{2^n}\left(A_0 + 2A_1 + 4A_2 + - - - + 2^{n-1}A_{n-1}\right) \qquad (1)$$

where, A_0, A_1, …, A_{n-1} are the bit values of the n-bit digital control word (N). Equation (1) can also be expressed as

$$V_2 = K_1 V_1 \qquad (2)$$

where, $K_1 = N/2^n$.

The equivalent of the Figure 1(a) is given in Figure 1(b) and now onwards shall be expressed as the K_1-Block. If two stages of the K_1- Block with same control word are cascaded through a voltage buffer as shown in Figure 1(c),

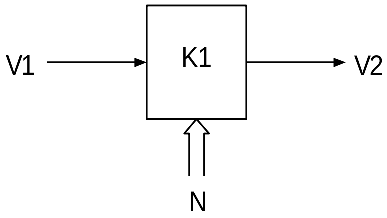

Fig 1(b): The K_1 – Block.

The transfer gain can be expressed as

$$\frac{V_2}{V_1} = K_2 \qquad (3)$$

where, $K_2 = K_1 K_1 = (N/2^n)^2$. Henceforththis double stageblock shall be referred as the K_2 – Block. Its equivalent is also shown in Figure1(c). It is obvious from equation (2) and (3) that the transfer gain of the K_1 and K_2 modules can be controlled through digital control word (N).

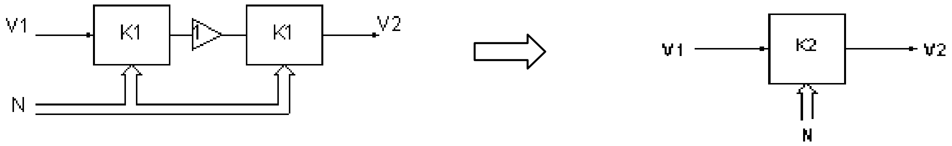

Fig. 1(c): The K_2 – Block

The j^th digital switch used in the DCM is shown in Figure 1(d), where, j ranges from 0 to n-1.

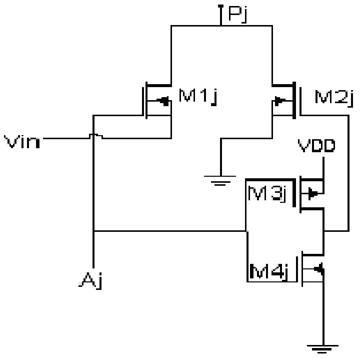

Fig. 1(d): The j^th Digital Switch.

III. CIRCUIT REALIZATION

The proposed DPGIM using a CCII and a DCM is given in Figure 2. The routine analysis yields its impedance function as

$$Z_{in} = \frac{V}{I} = \pm KZ \qquad \text{(4a)}$$

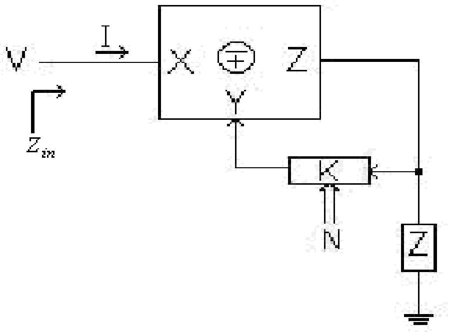

Fig. 2: DPGIM for positive impedance parameters

where, K (= N/2^n)is the transfer gain of the DCM and N is an n-bit control word. Thus, the realized impedance of equation (4) reduces to

$$Z_{in} = \pm\left(\frac{N}{2^n}\right)Z \quad (4b)$$

It is to be noted that for negative CCII the realized impedance Z_{in} is positive while for positive CCII, anegative Z_{in} is realized. From equation (4b) it is clear that the impedance seen at the input port of the Figure 2 can easily be controlled by digital word N, in turn the terminating impedance Z is controlled. The terminating impedance Z may be selected either resistor(R), capacitor (C) or inductor (L) or any combination of these components. Thus the circuit realizes digitally controlled positive as well as negative impedance multiplier

Case 1: **Digitally Programmable ± R**

In Figure 2, if Z is considered as resistor i.e., Z = R, equation (4) reduces to

$Z_{in} = R_e$ (5a)

For K = K_1

$$R_e = \pm\frac{N}{2^n}R \quad (5b)$$

and for K = K_2

$$R_e = \pm\left(\frac{N}{2^n}\right)^2 R \quad (5c)$$

It is can be seen from equation (5) that the realized effective resistance Re is programmable through digital control word N. For, K=K_1, R_e is directly related to the digital control word N, while for K=K_2, It is directly related to N^2.

Case 2: **Digitally Programmable ± C**

If Z in Figure 2 is assumed as capacitor i.e. Z = 1/sC, equation (4) reduces to

$$Z_{in} = \frac{1}{sC_e} \quad (6a)$$

For K = K_1

$$C_e = \pm\frac{2^n}{N}C \quad (6b)$$

while for K = K_2

$$C_e = \pm\left(\frac{2^n}{N}\right)^2 C \quad (6c)$$

Thus it is obvious from equation (6) that through digital control word (N), the realized effective capacitance(C_e) can be controlled inversely through N or N^2.

Case 3: **Digitally Programmable ± L**

In Figure 2 if Z is considered as an inductor i.e. Z = sL, equation (4) reduces to

$$Z_{in} = s\,L_e \quad (7a)$$

Again for K = K_1

$$L_e = \pm\left(\frac{N}{2^n}\right)L \quad (7b)$$

and for K = K_2

$$L_e = \pm\left(\frac{N}{2^n}\right)^2 L \qquad (7c)$$

Thus by controlling the digital control word N the realized effective inductance L_e is also programmable either through N or N^2.

IV. SIMULATION RESULTS

The practical validity of the proposed digitally programmable grounded impedance multiplier is simulated using PSPICE for ± R. The SPICE model of CCII available in the technical literature was used [2]. The digital control module of Figure (1) was implemented for 4-bit with W/L ratio of unity. The voltage - current plot obtained from PSPICE simulation for the DGPIM of Figure 2 with R=100KOhm for various N is shown in Figure 3(a).

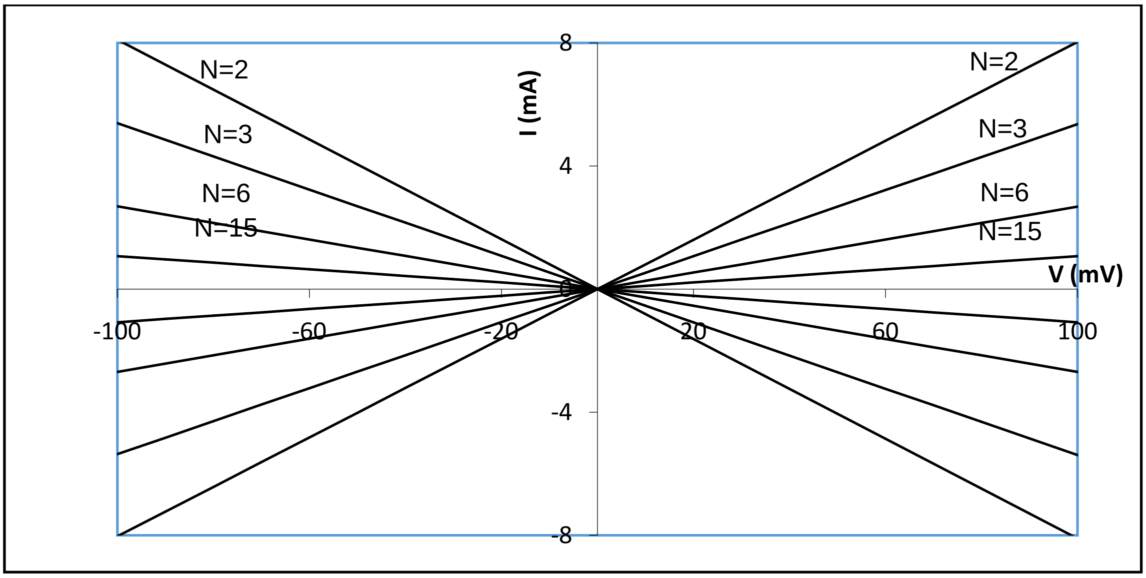

Fig. 3(a): V-I plot for digitally programmable positive and negative resistors for \ different digital control word N realized from the DPIM.

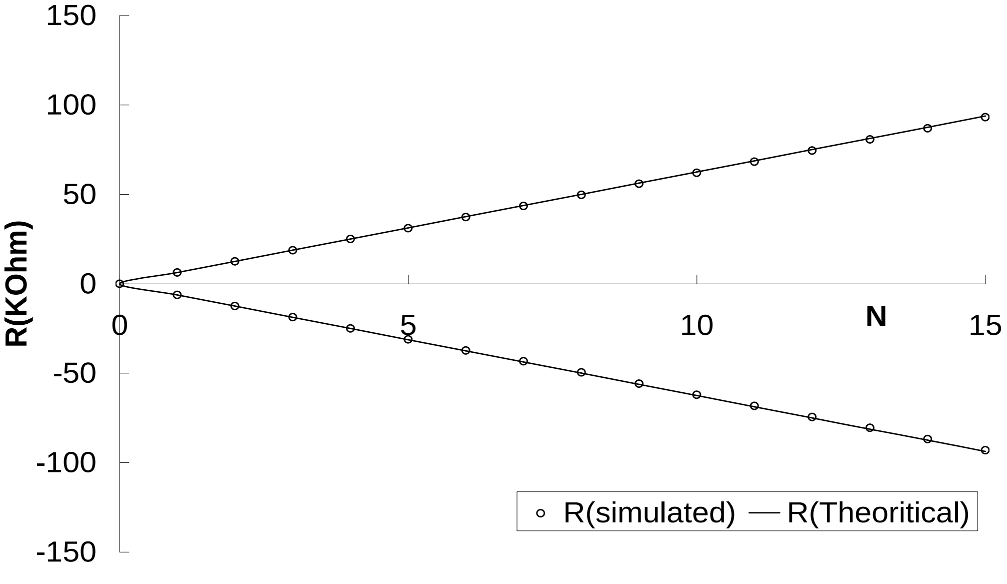

Fig. 3(b): Variation of R with N for positive and negative resistor.

Also, by varying the digital control word (N) the resistance ± R is controlled and the results obtained are shown in Figure 3b. The Figure 3 clearly exhibits the responses in close conformity with the design.

V. CONCLUSION

A digitally programmable impedance multiplier using CCII is presented. This impedance multiplier realizesdigitally controlled positive as well as negative grounded resistor, capacitor, and inductor. The technique used is simple versatile as well as compatible in contemporary IC technologies. It is to be noted that the digitally programmable circuit parameters in all the realizations are reconfigurable. The resolution of the digital control can be improved by using larger number of bits in the digital control module. The realized circuit was designed and simulated for ± R using PSPICE. The results thus obtained verify the theory.

REFERENCES

[1]. B. Wilson, (1992). Tutorial review: Trends in current conveyors and current mode amplifier design. Int. J. Electronics, 73(3), 573-583.
[2]. J. A. Svobodo, (1994). Transfer function syntheses using current conveyors. International Journal of Electronics, 76, 611-614.
[3]. I. A. Khan and Maheshwari, (2000). Simple first order all pass section single CCII. International Journal of Electronics, Vol. 87, No. 3, pp. 303 - 306.
[4]. H. Alzaher, (2006). CMOS digitally programmable inductance, ICM – 06, Saudi Arabia.
[5]. S. M. Al-Shahrani, and M. Al-Gahtani, (2006). A new poly-phase current-mode filter using digitally programmable current-controlled current-conveyor, ICM - 06, Saudi Arabia.
[6]. I. A. Khan, M. R. Khan and N. Afzal, (2006). Digitally programmable multifunctional current mode filter using CCIIs. Journal of Active and Passive Devices. Vol. 1, pp. 213-220.
[7]. V. Lakshminarayanan, (1997). Frequency programmable analogue based – pass filter. Electronics world, pp. 234 -237.