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A Novel Efficient VLSI Architecture Modified 16-B SQRT Carry Select Adder

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Abstract:- Duet advancement of new technology in the field of VLSI and Embedded system, there is an increasing demand of high speed and low power consumption processor. Speed of processor greatly depends on its multiplier as well as adder performance. Due to which high speed adder architecture become important. Sever a ladder architecture designs have been developed to increase the efficiency of the adder. In this paper, we introduce an architecture that performs high speed modified carry select adder using boot hen coder (BEC) Technique. Booth encoder, Mathematics is an ancient Indian system of Mathematics. Here we are introduced two carry select based design. These designs are implementation Xilinx Vertex device family.

Keywords:- Carry Select Adder (CSA),16-BSQRT CSA, Booth Encoder(BEC).

I. INTRODUCTION

Adders are commonly found in the critical path of many building blocks of micro processors, microcontroller, digital image processing and digital signal processing chips. Adders are essential not only for addition, but also for subtraction, multiplication, and division. Addition is one of the fundamental arithmetic operations. A fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders. The most important for measuring the quality of adder designs in the past were propagation delay, and area. In array processing and in multiplication and division, multi-operand addition is often encountered. More powerful adders are required which can add many numbers instead of two together. The design of a high-speed multi-operand adder called Carry Save Adder (CSA).A ripple carry adder turns into a carry-save-adder if the carry is saved (stored) rather than propagate

The name "carries save " arises from the fact that we save the carry-out word instead of using it immediately to calculate a final sum. The principal idea is that the carry has a higher power of 2 and thus is routed to the next column. Carry save adder is ideal to add several operands together. Thus, it can prevent time-consuming carry propagation and speed up computation. Effortthepastshowsthat16-bit CSA is the fastest adder with in other adders [WA Novel VLSI Architecture for FFT utilizing Proposed 4:2 & 7:2 Compressorang,Y. Pai,C.Song,X,1998]

II. BOOTHENCODER (BEC)

Booth encoding is a techniques to reduce the number of partial products inn-bit encoder. Booth encoder change the binary to excess-1converter is used to reduce the area and power consumption in CSA.

Figure1showsthebasicstructureof3-b BEC.TheBooleanexpressionsofthe3-bBECisas

X0= ~B0 (1)
X1=B0^B1 (2)
X2= B2^(B0&B1&B2) (3)

Table1: Function Table of 3-bit Booth Encoder

Binary[2:0]	Excess-1[2:0]
000	001
001	010
010	011
|	|
|	|
|	|
111	000

The main idea of booth encoder instead of the RCA with RCA (ripple carry adder) and C in=1in order to reduce the area and power consumption of the16-BSQRTCSA.

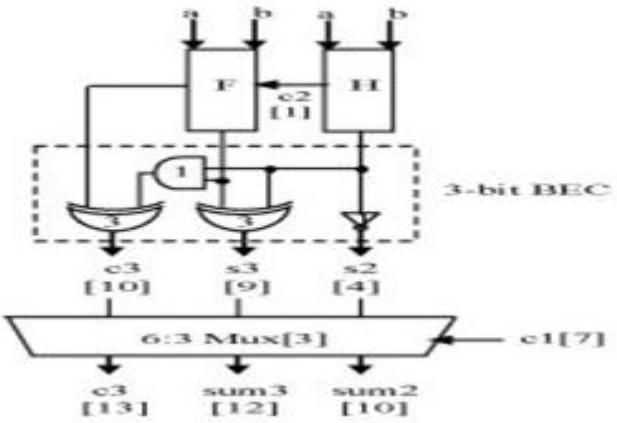

Figure 1:3-bit Booth Encoder

III. BASIC STRUCTURE OF 16-B SQRT CSA USING RCA AND BEC

Figure2 shows schematic of the 16-B SQRT CSA using BEC (Binary to excess-1 converter) instead of the RCA with cin = 1. The structure consists of five groups with different bit size RCA and BEC. Fig shows the group 2 of the CSA in details and calculation of area and power delay. The group 2 has one 2-B RCA which has1 full adder (FA) and 1half adder (HA) for Cin = 0 and a 3-B BEC is used instead of another 2-b RCA with Cin = 1. In similar manner the area and power delay can be calculated for each group.

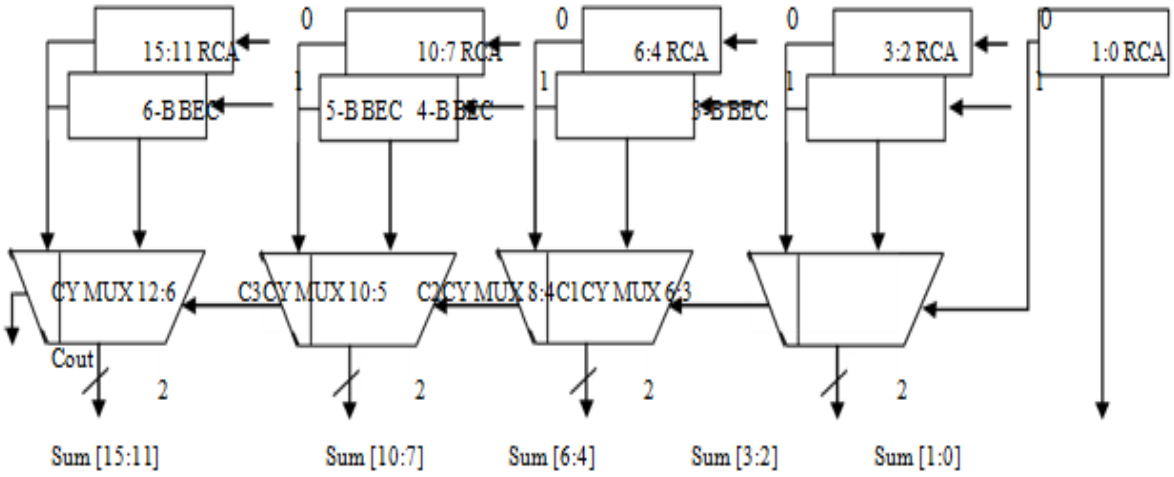

Figure 2: 16-B SQRT CSA. The parallel RCA with Cin=1 is replaced with BEC.

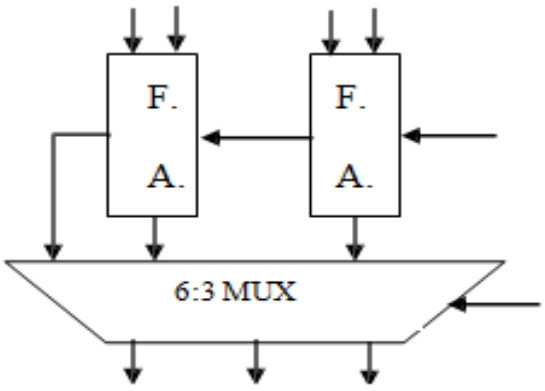

Figure 3: Basic structure of 6:3 MUX

IV. PROPOSED STRUCTURE OF 16-B SQRT CSA USING BEC

The structure of the proposed 16-B modified CSA using BEC for RCA with C_i □1isshowninFigure4Inthe proposed architecture we have replaced RCA with a BEC for C_i □1.Themainadvantageof this BEC logic comes from the lesser number of logicg attest an then-bit Full Adder(FA)structure.

The CSA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and the select a carry to generate the sum. However, the CSA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA)to generate partial sum and carry by considering carry input C_i □0and C_i □1, then the final sum and carry are selected by the multiplexers (mux)

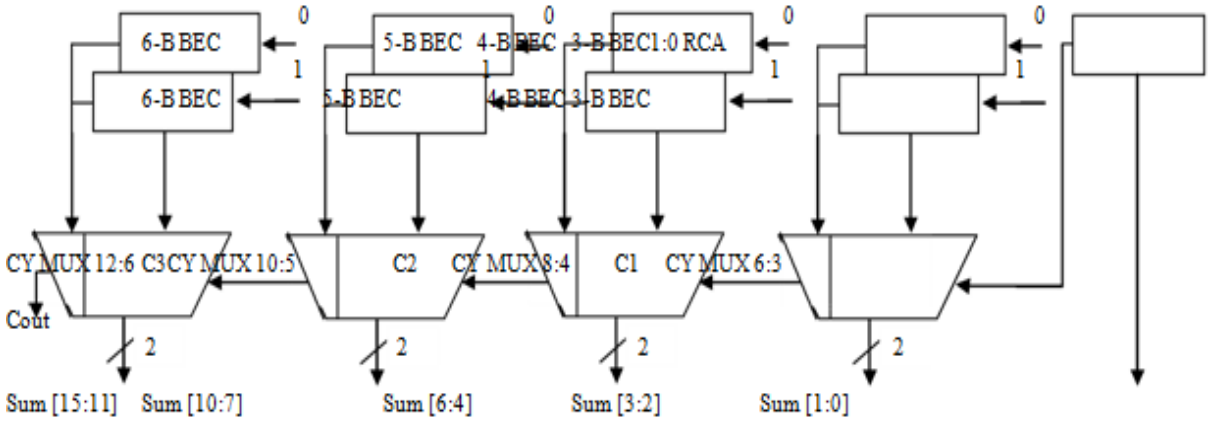

Figure 4: 16-B SQRT CSA using Booth Encoder (BEC)

Table2: Compared Result for16-BSQRTCS A using RCA and16-BSQRTCSA using BEC in Sparten 2DeviceFamily using

Design	Number of Slice	Number of bonded IOBs	4Input LUTs	Maximum Combination Path Delay
16-B SQRT CSA using RCA	30 out of 192	53 out of 180	53 out of 384	28.079ns
16-B SQRT CSA using BEC	25 out of 192	50 out of 180	45out of 384	24.940ns

Table 3: Compared Result for 16-B SQRT CSA using RCA and 16-B SQRT CSA using BEC in Vertex 2 Device Family using

Design	Number of Slice	Number of bonded IOBs	4Input LUTs	Maximum Combination Path Delay
16-B SQRT CSA using RCA	30 out of 192	53 out of 180	53 out of 384	14.79lns
16-B SQRT CSA using BEC	25 out of 192	50 out of 180	45out of 384	12.330ns

Table 4: Compared Result for 16-B SQRT CSA using RCA and 16-B SQRT CSA using BEC in Vertex E Device Family using

Design	Number of Slice	Number of Slice flip flops	4Input LUTs	Maximum Combination Path Delay
16-B SQRT CSA using RCA	226	36	384	26.635ns
16-B SQRT CSA using BEC	69	36	113	22.001ns

All the designing and experiment regarding algorithms have been captured by VHDL and the functionality is verified by RTL and gate level simulation. Comparison result for proposed design in Vertex E device family in has shown the Table1, Table2 andTable3 respectively.

V. CONCLUSION AND FUTURESCOPE

We studied about different adders among compared them by different criteria like number of slice and Times of that we can judge to know which adder was best suited for situation. After comparing all we came to a conclusion that Carry Select Adders are best suited for situations where Speed is the only criteria. Similarly Ripple Carry Adders are best suited for Low Power Applications. But Among all the Carry Select Adder had the least Area-Delay product that tells us that, it issue table for situations where both low power and fastness area criteria such that we need a proper balance between both as is the case with our Paper.

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