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Minimization of Losses in Distribution Systems for the Improvement of Power Quality by Using UPFC

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Abstract—Minimization of line losses and the improvement of power quality in distribution system are the most challenging problems, particularly when it is not economic to upgrade the entire feeder systems. This paper presents a new method to achieve the line loss minimum condition and improve power quality in radial and loop distribution system by using Unified Power Flow Controllers (UPFC), one of the most important FACTS devices. For regulating voltage using PWM controllers and to minimize losses in distribution systems. First, the line loss minimum conditions in distribution systems are present then load voltage regulation is applied under line minimum condition to improve the power quality. Reference voltage of the controlled node is determined based on the assumptions that this voltage can subsequently improve all node voltages to be with in the permissible range.

Keywords—Loop distribution system, series compensation, unified power flow controller (UPFC), power quality, voltage regulation, line loss minimization.

I. INTRODUCTION

Now-a-days there are different power quality issues and power problems each of which might have varying and diverse causes. Among all power quality issues, voltage drop is the most severe one that can lead to tremendous losses to the customers. Therefore, voltage is one of the most important elements of the electric power quality. If the Power Quality of the network is good, then any loads connected to it will run satisfactory and efficiently. If the Power Quality of the network is bad, then loads connected to it will fail or will have a reduced lifetime, and the efficiency of the electrical installation will reduce.

Flexible AC transmission systems (FACTS) controllers have been mainly used for solving various power system steady state control problems. However, recent studies reveal that FACTS controllers to improve the power quality and to minimize losses. The concept of Flexible AC Transmission System (FACTS) was introduced as a family of power electronic equipments which have emerged for controlling and optimizing flow of electrical power in the distribution lines. In addition, many papers considering loss reduction and improvement of power quality in distribution systems, using FACTS devices, have been published. Most of them used STATCOM, shunt active filter, series-shunt power converter, and BTB converter to regulate and balance load voltages and to reduce line loss by reactive power injection. However, these literatures did not consider minimization of line loss and improving power quality.

This paper presents minimum conditions for the losses in distribution systems and experimentally achieved them by using unified power flow controllers (UPFC). Among the FACTS components, Unified Power Flow Controller (UPFC) is the most complete. It is able to control independently the throughput active and reactive powers. The UPFC is capable to act over three basic electrical system parameters: line voltage, line impedance, and phase angle, which determine the power.
There are three basic types of distribution system designs: Radial, Loop, or Network. The Radial distribution system is the cheapest to build, and is widely used in sparsely populated areas. A radial system has only one power source for a group of customers. A power failure, short-circuit, or a downed power line would interrupt power in the entire line which must be fixed before power can be restored.

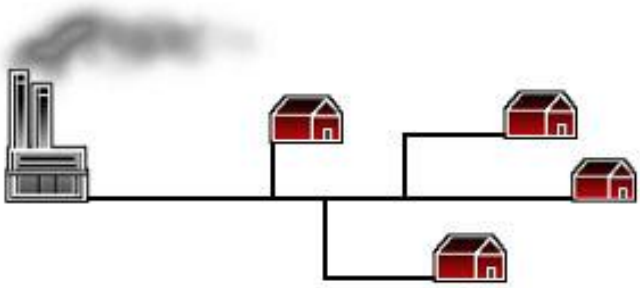

Fig.1 Radial distribution system

A loop system, as the name implies, loops through the service area and returns to the original point. The loop is usually tied into an alternate power source. By placing switches in strategic locations, the utility can supply power to the customer from either direction. If one source of power fails, switches are thrown (automatically or manually), and power can be fed to customers from the other source. The loop system provides better continuity of service than the radial system, with only short interruptions for switching. In the event of power failures due to faults on the line, the utility has only to find the fault and switch around it to restore service. The fault itself can then be repaired with a minimum of customer interruptions. The loop system is more expensive than the radial because more switches and conductors are required, but the resultant improved system reliability is often worth the price.

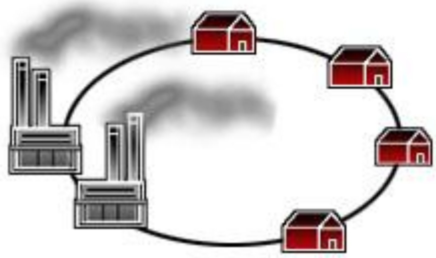

Fig.2 loop distribution system

Network systems are the most complicated and are interlocking loop systems. A given customer can be supplied from two, three, four, or more different power supplies. Obviously, the big advantage of such a system is added reliability. However, it is also the most expensive. For this reason it is usually used only in congested, high load density municipal or downtown areas.

II. UNIFIED POWER FLOW (UPFC) CONCEPT

The UPFC configuration is shown in fig3.

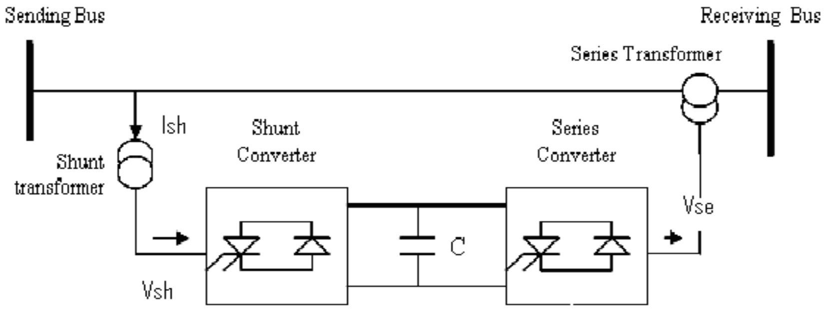

Fig.3 Basic Structure of an UPFC

It can be seen that the UPFC consists of a series and a shunt converter is connected back-to-back through a common dc link. The shunt converter is connected also in parallel with the line transmission by transformer, allows controls the UPFC bus Voltage/shunt reactive power and the dc capacitor voltage

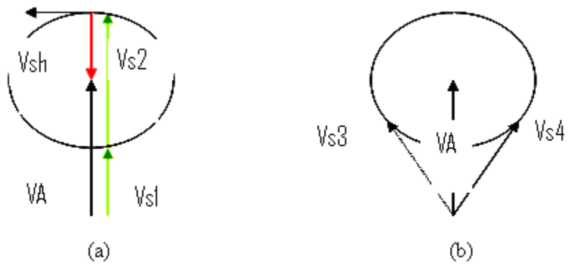

Fig.4. Power exchange of the Shunt Converter

Figure 4(a) shows the exchange of the reactive power between the UPFC and the electrical system. The shunt converter generates a voltage Vs1 in phase with VA but with variable magnitude. If Vs=Vs1. The UPFC injects some reactive power, if Vs=Vs2 the UPFC absorbs some reactive power and no reactive power is exchanged for Vs=VA. In order to compensate the series converter losses, figure 3b shows very clearly. That the active power is exchanged between UPFC and the electrical system. The Voltage generated by shunt converter is no it in phase with the voltage of the system but of the same magnitude. Whereas the series converter of the UPFC controls the transmission line real/reactive power flows by injecting a series voltage of adjustable magnitude and phase angle. The UPFC can provide multiple power flow control functions by adding the injected voltage phasor with appropriate magnitude V_{se} and phase angle to the sending-end-voltage phasor.

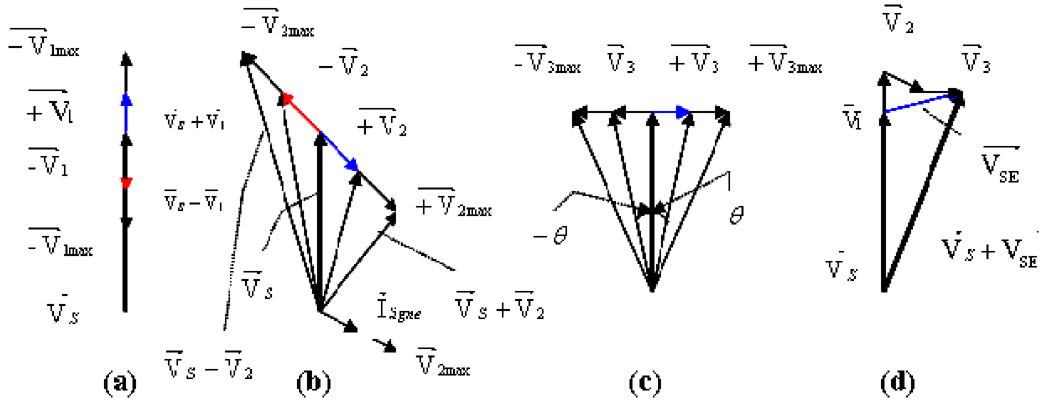

Fig. 5 Series Voltage Injected Phasor diagrams.

As illustrated in figure 4, by the appropriate choice (control) of phasor V_{se}, the three customary power flow control functions:
1) Voltage regulation
2) Series reactive compensation.
3) Phase Shift.
Simultaneous control of terminal voltage, line impedance and phase angle allows the UPFC to perform multifunctional power flow control.

III. MINIMIZATION CONDITIONS FOR LINE LOSS

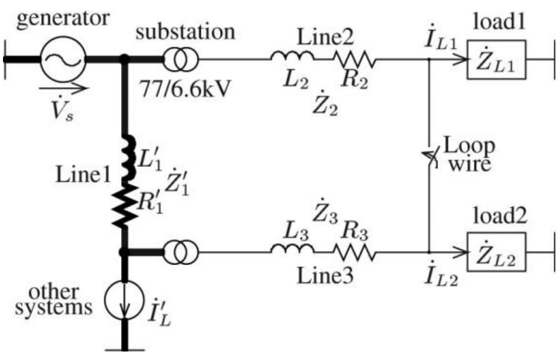

Fig.6 Model of distribution system.

Fig. 6 shows a simple model of the distribution system. In this model, impedances of lines 1, 2, and 3 are $Z_1 = R_1 + j\omega L_1$, $Z_2 = R_2 + j\omega L_2$, and $Z_3 = R_3 + j\omega L_3$, respectively. The load impedances are ZL_1 and ZL_2. The other systems, connected to this system, are represented by a current source. The system is reconfigured to be loop system by connecting the adjacent ends of line 2 and line 3, using loop wire. The load currents I_{L1} and I_{L2} and the other systems current I_L are assumed to be constant. Also, the line currents I_{0i} (i=1, 2, 3, and 4) flow in each line in the same direction (counter clockwise). According to the line currents and the system parameters, the total line loss P_l in the loop system can be formulated as follows:

$$
\begin{aligned}
P_l &= \sum_{i=1}^{3} R_i |\dot{I}_{0i}|^2 \\
&= R_{\text{loop}} \left| \dot{I}_{01} - \frac{R_2 \dot{I}_{L1} + R_2 \dot{I}_{L2} + (R_2 + R_3)\dot{I}_L}{R_{\text{loop}}} \right|^2 \\
&\quad - \frac{|R_2 \dot{I}_{L1} + R_2 \dot{I}_{L2} + (R_2 + R_3)\dot{I}_L|^2}{R_{\text{loop}}} \\
&\quad + R_2 |\dot{I}_{L1} + \dot{I}_{L2} + \dot{I}_L|^2 + R_3 |\dot{I}_L|^2 \qquad (1)
\end{aligned}
$$

where

$$R_{\text{loop}} = \sum_{i=1}^{3} R_i . \qquad (2)$$

Since the second, third, and fourth parts in (1) are constants, because the currents I'_{L1}, I'_{L2}, and I_L are assumed to be constants, the first part is the only part that can be used to obtain the line loss minimum conditions. These conditions can be obtained by equating the first part in (1) with zero. In this case, the total line loss $P_{l\min}$ in loop system can be formulated as follows:

$$P_{l\min} = \sum_{i=1}^{3} R_i \left| \dot{I}_{mi} \right|^2 \qquad (3)$$

Where $\dot{I}_{mi}$ (i = 1, 2, and 3) is the line current that flows in the loop lines in case of line loss minimization. The loss minimum line currents can be formulated as follows:

$$\left.\begin{aligned} \dot{I}_{m1} &= \frac{R_2\dot{I}_{L1} + R_2\dot{I}_{L2} + (R_2+R_3)\dot{I}_L}{R_{\text{loop}}} \\ \dot{I}_{m2} &= -\frac{(R_1+R_3)\dot{I}_{L1} + (R_1+R_3)\dot{I}_{L2} + R_1\dot{I}_L}{R_{\text{loop}}} \\ \dot{I}_{m3} &= \frac{R_2\dot{I}_{L1} + R_2\dot{I}_{L2} - R_1\dot{I}_L}{R_{\text{loop}}} \end{aligned}\right\}. \qquad (4)$$

The difference between the currents I_{0i} and I_{mi} is defined as the loop current I_{loop} that circulates in loop system in the same direction, and can be formulated as follows:

$$\dot{I}_{\text{loop}} = \dot{I}_{0i} - \dot{I}_{mi} = -\frac{\sum_{i=1}^{3} j\omega L_i \dot{I}_{0i}}{R_{\text{loop}}}. \qquad (5)$$

The line loss minimum conditions in loop systems can be realized by eliminating the loop current I_{loop} from the system, which can be achieved if any of the following conditions, is realized:

$$\frac{R_1}{L_1} = \frac{R_2}{L_2} = \frac{R_3}{L_3} \qquad (6)$$

$$\sum_{i=1}^{3} j\omega L_i \dot{I}_{0i} = 0. \qquad (7)$$

IV. IMPROVEMENT OF POWER QUALITY UNDER LINE LOSS MINIMUM CONDITION

To improve the power quality voltage regulation is the main important one. Load voltage regulation problems in distribution systems are commonly solved by using STATCOM, which has the ability to control voltage magnitude by compensating reactive power. However, STATCOM cannot control the line loss in loop distribution systems. On the other hand, series compensators, such as UPFC, have the ability to regulate load voltage, to minimize line loss and improve power quality simultaneously in the radial and loop distribution system. The main object of this paper is to minimize the total line loss and to regulate the load voltages in loop distribution system, simultaneously. The line loss minimum conditions can be achieved if the loop current is eliminated from the loop system. Under this condition, the load voltages can be controlled in order to keep it within the permissible voltage range, ±5% of the nominal source voltage. Fig. 7 shows a simple model of the loop distribution system that is used to simplify the idea of power quality under line loss minimum condition. In this model, V_s, V_1, and V_r are assumed to be source voltage, load 1 voltage, and (loads 2 and 3) voltage, respectively. The series voltage source V_c is assumed to be a controlled series voltage that is used to regulate the load voltages. The controlled series voltage V_c is inserted to the loop system by the UPFC series converter. Therefore, the voltage V_c is assumed to be controlled in both voltage magnitude and phase angle.

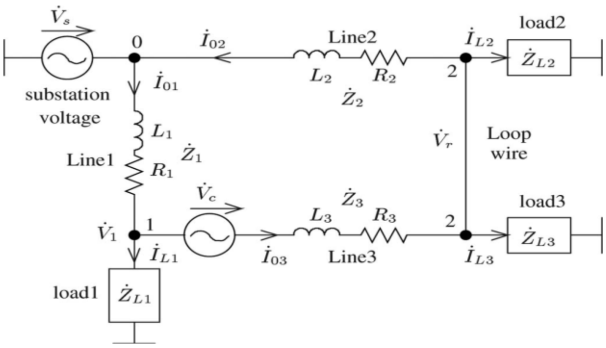

Fig.7 Model of loop distribution system with series voltage source.

A. Before Installing the Controlled Series Voltage V_c

Fig. 8(a) shows the phasor diagram of the line currents and node voltages in the loop system shown in Fig. 7. The permissible voltage range is defined by the lower and upper voltage limits. It is cleared that the node 2 voltage *Vr* is less than the lower voltage limit and lags behind the source voltage *Vs* by the angle *θ*. Therefore, series compensation can be used to control node 2 voltage in order to regulate all node voltages to be within the permissible voltage limit.

B. After Installing the Controlled Series Voltage □Vc

Installing a series voltage source in a loop distribution system affects the power flow and hence changes all the node voltages. Based on the superposition theorem, the change in node 1 and node 2 voltages due to the installation of the controlled series voltage ˙*Vc* in the loop system shown in Fig. 3 can be formulated as follows:

$$\left.\begin{aligned}\Delta\dot{V}_1 &= -\dot{V}_c\frac{\dot{Z}_1}{\dot{Z}_{\text{loop}}}\\ \Delta\dot{V}_r &= \dot{V}_c\frac{\dot{Z}_2}{\dot{Z}_{\text{loop}}}\end{aligned}\right\} \quad (8)$$

where V_c is the series injected voltage, and Z_{loop} is the summation of the loop impedances. Fig.8(b) and (c) shows the phasor diagrams of all line currents and node voltages after installing the controlled series voltage V_c. The phasor diagrams are drawn based on the change in each node voltage due to the installation of V_c. The value of the controlled series voltage ˙*Vc* is determined according to its function in the loop distribution system, and the change in each node voltage can be calculated based on (8).

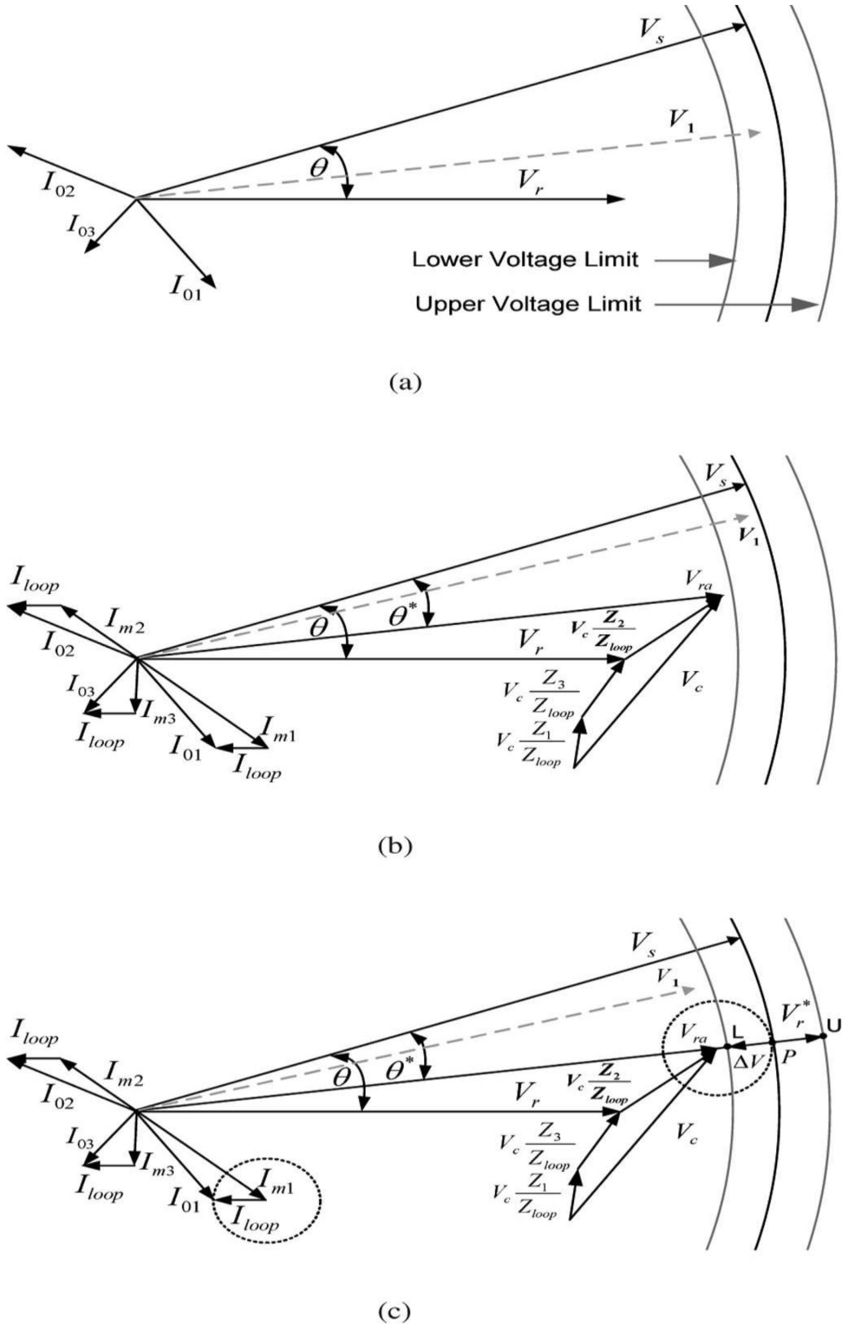

Fig. 8. Phasor diagram of the loop distribution system. (a) Before installing ˙V_c (b) After installing ˙*V c* to achieve line loss minimization. (c) After installing V_c to achieve voltage regulation under line loss minimization.

Since the controlled series voltage V_c realize its function by controlling the node 2 voltage, the phasor lines, representing the change in each node voltage, are drawn to show the overall change related to node 2 voltage. Also, the line currents I_{0i} and their components (I_{mi} and I_{loop}) are drawn in the phasor diagrams based on (4) and (5). The focus of the phasor diagrams, shown in Fig. 8(b) and (c), is the relation between the change in the node 2 voltage and the loop current. In the system shown in Fig. 7, if the controlled series voltage V_c is installed to achieve loss minimum condition, node 2 voltage changes to be V_{ra} , which is still less than the lower voltage limit and lags behind source voltage V_s by the angle $\theta*$, as shown in Fig. 4(b). In this case, node 2 voltage can be formulated as follows

$$\dot{V}_{ra} = \dot{V}_r + \dot{V}_c \frac{\dot{Z}_2}{\dot{Z}_{\text{loop}}} \qquad (9)$$

where V_r is the load voltage before installing V_c , and V_{ra} is the load voltage after installing V_c . Inserting a controlled series voltage in loop system to achieve line loss minimization affects all voltages in the system. However, Fig. 8(b) shows that this method cannot guarantee all node voltages to be within the permissible voltage range.
Fig. 4(c) shows the phasor diagram of the distribution system, shown in Fig. 3, with the effect of using V_c to achieve load voltage regulation under line loss minimum condition. Based on the loop current, total power loss shown in (1) can be formulated as follows:

$$P_l = \sum_{i=1}^{3} R_i|\dot{I}_{0i}|^2 = \sum_{i=1}^{3} R_i|\dot{I}_{mi}|^2 + R_{\text{loop}}|\dot{I}_{\text{loop}}|^2. \qquad (10)$$

Equation (10) shows that any circle centered by the current I_{mi} , due to the change in loop current, has constant power loss. The change in loop current will change the node 2 voltage by ΔV , as shown in Fig. 8(c). The resultant node 2 voltage can be formulated as follows:

$$\left.\begin{aligned} \dot{V}_r^* &= \dot{V}_{ra} + \Delta\dot{V} \\ \Delta\dot{V} &= \dot{Z}_2 \dot{I}_{\text{loop}} \end{aligned}\right\}. \qquad (11)$$

Equation (11) shows that changing the loop current to draw a circle around its center $\dot{I}mi$ causes the node 2 voltage to draw a similar circle around its center $\dot{V}ra$ that also has constant power loss. In case of line loss minimization, the loop current is zero and hence the radius of both circles is zero. As the loop current increases, the radius of these circles and hence total line loss increase, too. The tangential point, point (P), between the circle centered by $\dot{V}ra$ and the circle of source voltage loci, represents the point, at which node 2 voltage equals in magnitude to source voltage under loss minimum condition. In general, controlling node 2 voltage to be lag behind Vs by the angle $\theta*$, means controlling the voltage under line loss minimum condition. However, controlling the node 2 voltage to be equal in magnitude to source voltage under line loss minimum condition cannot guarantee all node voltages to be within the permissible voltage range. According to (8), the change in node 2 voltage causes an opposite change in the node 1 voltage, that may cause the node 1 voltage to be less than the lower voltage limit.

In this paper, the reference magnitude of node 2 voltage is controlled to be in between points *L* and *U*, as shown in Fig. 8(c), in order to achieve all node voltages within the permissible voltage range under line loss minimum condition. The reference magnitude will start at point (p), then changes toward point (L) or (U) according to the voltage at node 1 in order to realize all node voltages in between the permissible voltage limit.

V. PROPOSED CONTROL SCHEME

The proposed control scheme has been developed to meet the following objectives, simultaneously: 1) minimize total power loss in loop distribution systems; and 2) regulate all node voltages to be within permissible voltage range to improve power quality.

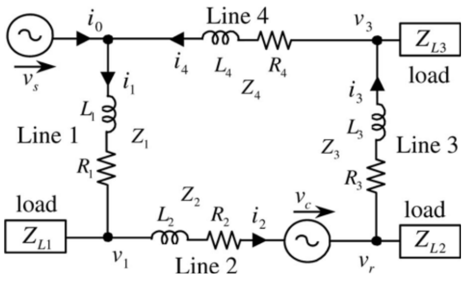

Fig.9 Model of the system in case study.

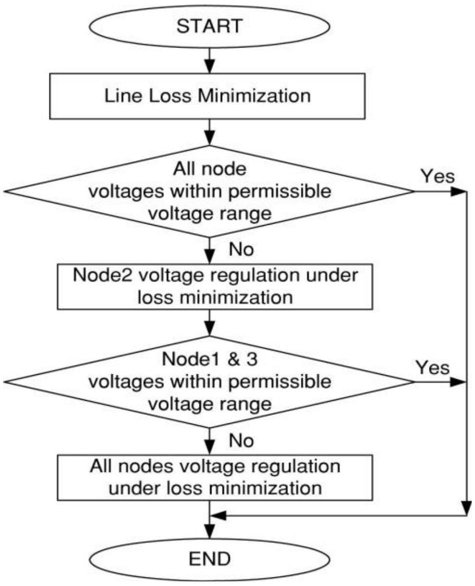

Fig.10 Control steps of UPFC series converter.

Fig. 9 shows the loop distribution system model controlled by the UPFC. In this model, the UPFC series converter is represented by series voltage source connected at line 2, whereas the shunt converter is disregarded because its current is not as large as the distribution line current. The distribution system model has three nodes that their voltages can be controlled by the UPFC. Fig. 10 shows the control flow chart of the UPFC series converter. First, the reference voltage of the UPFC series converter is calculated based on the line loss minimum condition. If any node voltage is outside the permissible voltage limit, UPFC will control the node 2 voltage to be equal in magnitude to the source voltage under line loss minimization. In this case, if the voltage at nodes 1 or 3 is still out of the limit, node 2 voltage magnitude will be controlled in order to keep them within the limit. In all cases, the reference angle of node 2 voltage is $\theta*$ to control the node voltages under loss minimization.

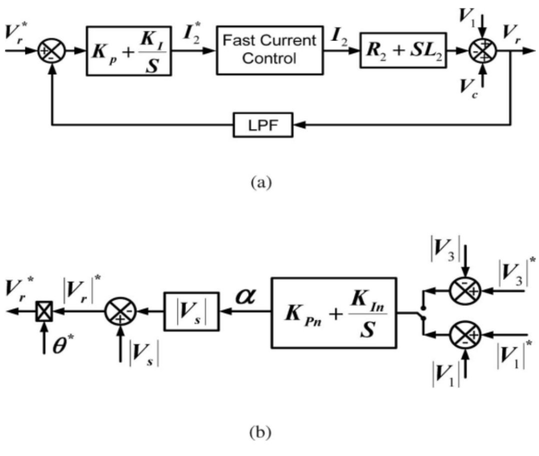

Fig. 11. Control scheme of UPFC series converter. (a) Main block control circuit. (b) Node voltage limit control.

Fig. 11 shows the proposed control block diagram of the UPFC series converter to achieve all nodes voltage regulation under line loss minimization by controlling node 2 voltage. The difference between reference and actual node 2 voltage is controlled by using proportional-integral (PI) controller to obtain the reference current of the UPFC line (line 2), which is used to calculate the reference voltage of UPFC series converter *Vc*. The parameters in control block diagram are transformed from three-phase axis to the *p*–*q* axes using Park–Clarke transformation. Also, the control technique used in this paper does not require any data about the loads because in practical distribution systems, loads are continuously varying. In order to achieve line loss minimization in the loop system, node 2 reference voltage can be formulated as follows:

$$\dot{V}_r^* = \|V_{ra}|\angle\theta^*. \qquad (12)$$

Reference voltage for loss minimization can be calculated by using the line currents that flow in loop lines under loss minimum condition (I_{mi}, (i = 1, 2, 3, and 4)) and the line parameters. In order to calculate these currents, first the UPFC circulating current, $I^{\cdot}_{\mathrm{UPFC}}$, is calculated as follows:

$$\dot{I}_{\mathrm{UPFC}} = \left| \frac{\dot{V}_c}{\dot{Z}_{\mathrm{loop}}} \right. . \qquad (13)$$

The line currents that flow in the loop system lines before installing UPFC (I_{0i}, [i = 1, 2, 3, and 4)] can be estimated by subtracting the UPFC circulating current, as shown in (13), from the loop system line currents as follows:

$$\dot{I}_{0i} = \dot{I}_i - \dot{I}_{\mathrm{UPFC}}. \qquad (14)$$

By using the currents I_{0i} , shown in (14), the loop current can be calculated as in (5). The line currents that flow in loop lines under loss minimum condition [*Imi*, (i = 1, 2, 3, and 4)] can be calculated as follows:

$$\dot{I}_{mi} = \dot{I}_{0i} - \dot{I}_{\mathrm{loop}}. \qquad (15)$$

By using the currents *Imi*, shown in (15), and the line parameters, the load voltage V_{ra} , and hence, the phase shift angle $\theta*$ can be calculated from the *p–q* axes components of *Vra* as follows:

$$\begin{aligned} \dot{V}_{ra} &= \dot{V}_s - \dot{Z}_1 \dot{I}_{m1} + \dot{V}_c - \dot{Z}_2 \dot{I}_{m2} \\ &= \dot{V}_s + \dot{Z}_4 \dot{I}_{m4} + \dot{Z}_3 \dot{I}_{m3} \end{aligned} \qquad (16)$$

$$\theta^* = \tan^{-1}\left(\frac{V_{raq}}{V_{rap}}\right). \qquad (17)$$

If the series injected voltage, for line loss minimization, cannot guarantee all node voltages to be within the permissible voltage limit, node 2 voltage magnitude should be controlled in order to achieve all node voltages within the limit. First, node 2 reference voltage is controlled to be equal in magnitude to source voltage and lag behind it by the angle $\theta*$ as follows

$$\dot{V}_r^* = |V_s| \angle \theta^*. \qquad (18)$$

$$V_c^* = (V_r^* - V_r)\frac{Z_{\mathrm{loop}}}{Z_3 + Z_4} \qquad (19)$$

$$I_{\mathrm{UPFC}} = \frac{V_c^*}{Z_{\mathrm{loop}}}. \qquad (20)$$

In the node 2 voltage before installing UPFC, *Vr*, is calculated using line currents [I_{0i}, (i = 1, 2, 3, and 4)], shown in (14). The estimated currents that flow in the loop system lines in case of controlling node 2 voltage, as in (18), are calculated by adding the circulating current shown in to the line currents [I_{0i}, (i = 1, 2, 3, and 4)], and the resultant line currents are used to calculate the estimated voltages at nodes 1 and 3. If the series injected voltage still cannot guarantee voltages at nodes 1 and 3 to be within the permissible voltage limit, an additional block diagram can be used in order to keep all node voltages within the limit, as shown in Fig. 7(b). The inputs of this additional block diagram can be node-1 or node-3 voltage, depending on which one of them is out of the limit. The reference values of nodes 1 and 3 voltages can be the lower or the upper voltage limits according to the value of node voltage. In this case, node 2 reference voltage can be formulated as follows:

$$V_r^* = |V_s|\,(1-\alpha)\,\angle\theta^* \qquad (21)$$

where α is the voltage limit controller.

VI. EXPERIMENTAL SYSTEM CONFIGURATION

A. Distribution System Configuration

In order to demonstrate the effectiveness of using UPFC to realize all nodes voltage regulation and total line loss minimization in the loop distribution systems simultaneously, a simple laboratory model of the distribution system is used. Fig. 12 shows the 230-V, 6-kVA laboratory model including the distribution system and the UPFC. The distribution system consists of four sets of three-phase lines, lines 1, 2, 3 and 4. First, the system works as two radial feeders which are fed from the same voltage source. Then, by using the loop wire to connect nodes *V2a* and *V2b* in parallel, the system is reconfigured to work as loop system with same line parameters. Installing loop wire makes the two node voltages *V*2*a* and *V2b* as one, known as *Vr*. The parameters of the whole system are listed in Table I.

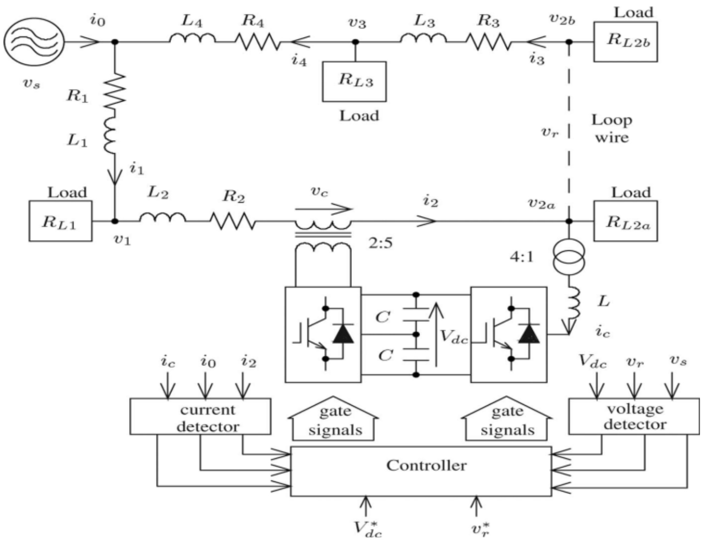

Fig.12 Experimental system configuration.

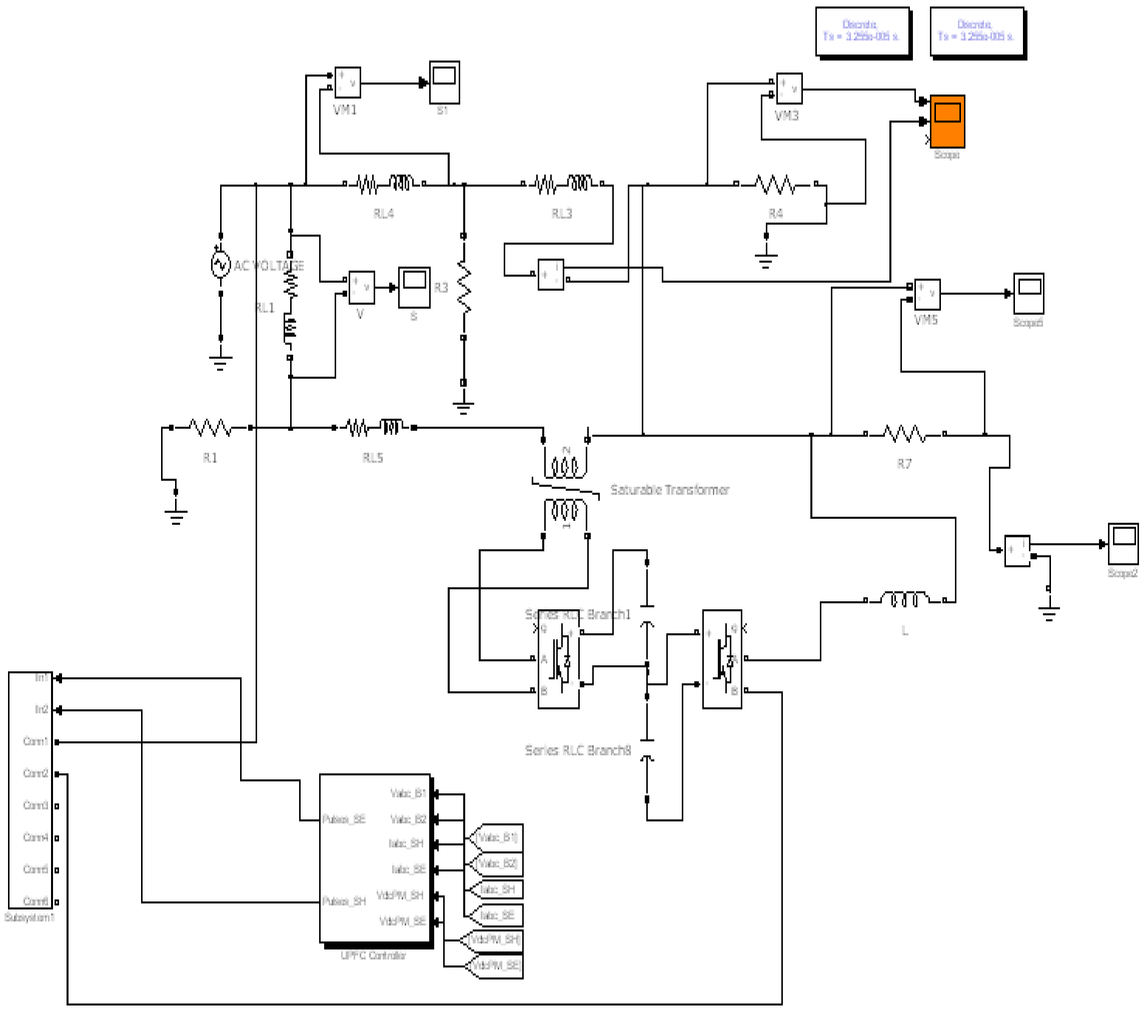

Fig.13 Simulation model

TABLE I : SYSTEM PARAMETERS (200 V–6 KVA BASE)

Source voltage v_s	203 V, 60 Hz
Load R_{L1}	30 Ω (0.22 p.u.)
R_{L2a}	80 Ω (0.08 p.u.)
R_{L2b}	26.7 Ω (0.25 p.u.)
R_{L3}	60 Ω (0.11 p.u.)
Line 1 L_1	6.0 mH (0.34 p.u.)
R_1	0.6 Ω (0.09 p.u.)
Line 2 L_2	6.0 mH (0.34 p.u.)
R_2	0.8 Ω (0.12 p.u.)
Line 3 L_3	6.0 mH (0.34 p.u.)
R_3	1.2 Ω (0.18 p.u.)
Line 4 L_4	6.0 mH (0.34 p.u.)
R_4	1.2 Ω (0.18 p.u.)
Capacitor C	3000 μF
Input L of shunt conv.	2.0 mH
DC link voltage V_{dc}	100 V
Switching time T_s	204 μs
Main PI gains K_p, K_I	10 A/V, 20 A/V.sec
Voltage limit PI gains K_pn, K_In	0.2 A/V, 0.3 A/V.sec

B. UPFC Circuit *Configuration*

Fig. 14 shows the configuration of UPFC used in the experimental system. It consists of combined series and shunt converters connected BTB to each other through a common dc-link capacitors. The series converter, which acts as a controllable voltage source *vc* , is used to inject a controlled voltage in series with the distribution line, and thereby to force the power flow to a desired value. The shunt converter, which acts as a controllable current source *ic* , is used to regulate the dc-link voltage by adjusting the amount of active power drawn from the distribution line to meet the real power needed by the series converter. In addition, the shunt converter has the capability of controlling reactive power.

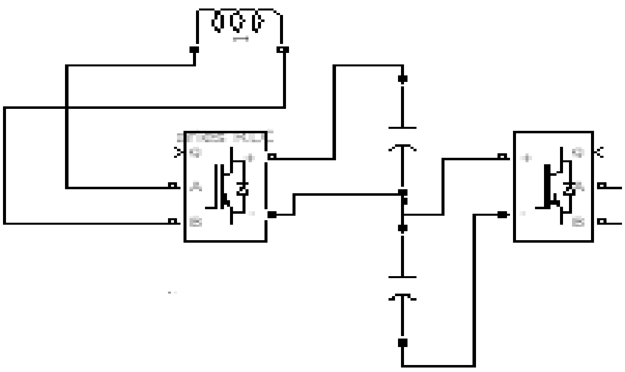

Fig.14 Simulation model for UPFC

TABLE II : EXPERIMENTAL RESULTS BEFORE AND AFTER INSTALLING UPFC

		Before UPFC		After UPFC		
		Radial	Loop	Case (1)	Case (2)	Case (3)
I_1	$[A]$	5.25	6.19	7.24	8.01	7.79
I_2		1.43	2.43	3.38	4.15	3.84
I_3		3.88	3.16	2.08	2.05	1.89
I_4		5.76	4.92	3.87	3.53	3.53
I_{loop}		0.0	1.13	0.04	1.32	0.85
V_s	$[V]$	203.0	203.0	203.0	203.0	203.0
V_1		196.6	193.5	193.9	187.6	190.1
V_{2a}		194.7	187.5	189.1	200.2	196.5
V_{2b}		180.3	187.5	189.1	200.2	196.5
V_3		188.9	192.5	193.6	198.6	197.2
V_c	$[V]$	0.0	0.0	11.5	18.5	15.2
P_{loss}	$[W]$	228.3	206.2	191.2	216.8	202.3

The UPFC series and shunt converters, shown in Fig. 8, have been built as a three-phase pulse width modulation (PWM) converter with insulated gate bipolar transistor (IGBT) SKM100GB124D as the power device. TheDSP TMS320VC33 is selected as the controller for both converters. The shunt converter is connected in parallel with the distribution line via a three-phase transformer. The series converter, multilevel converter, consists of three single-phase H-bridge converters. The ac terminals of each H-bridge converter are connected in series with the distribution line through a single-phase transformer. The switching and sampling frequencies for series and shunt converters are 2.45 and 4.9 kHz, respectively. The main function of the UPFC series converter is to realize all nodes voltage regulation and line loss minimization in the loop distribution system, simultaneously. Controlling the loop system by using UPFC requires detecting all line currents flowing in the loop lines, which in practical distribution system seems to be difficult. In the authors have proposed a new method for estimating all line currents and voltages in four lines loop system, and applied this method to achieve total line loss minimization. In this method, the detected signals are UPFC line current I_2 and node voltage Vr , in addition to the main source voltage Vs and its injected current I_0 . The currents ic , i_0 , and i_2 are detected by using normal current sensors. Also, the voltages V_{dc}, Vr , and Vs are detected by using normal voltage sensors. The outputs of the current and voltage sensors are connected to the AD converters in order to use in the DSP controller.

VII. EXPERIMENTAL RESULT

The laboratory model of radial and loop distribution system shown in Fig. 8 is carried out before and after installing UPFC. In each case, line currents, all node voltages, and power loss in each line are measured and listed in Table II for comparison. All line currents, voltages, and total power loss, shown in Table II, are measured by using the Digital Power Meters (Yokogawa WT1600) that are simultaneously connected in the sending and receiving ends of each line in the experimental system. The power loss in each line is calculated from the difference between the sending and receiving powers

A. Before Installing UPFC

The laboratory model shown in Fig. 12 is carried out first as two radial feeders fed from the same voltage source. Then, the system works as loop by connecting nodes *V*2*a* and *V*2*b* in parallel using loop wire. Installing loop wire makes the two node voltages *V*2*a* and *V*2*b* as one, known as *Vr* . Table II shows the experimental results of all line currents, loop current, all node voltages, and total line loss in the radial and loop configurations. In the radial configuration, node voltages *V*3 and *V*2*b* are less than the lower voltage limit (190 V). Although reconfiguring the system to work as loop one enhances the loop wire voltage *Vr* , it is still less than the lower voltage limit.

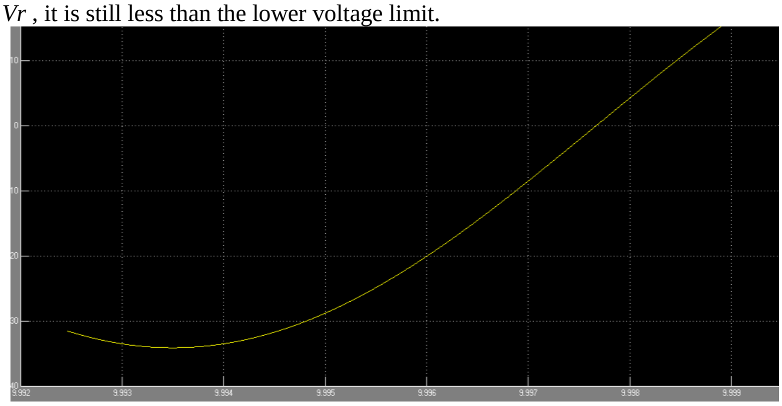

Fig. 15 experimental wave before installing upfc for loop system

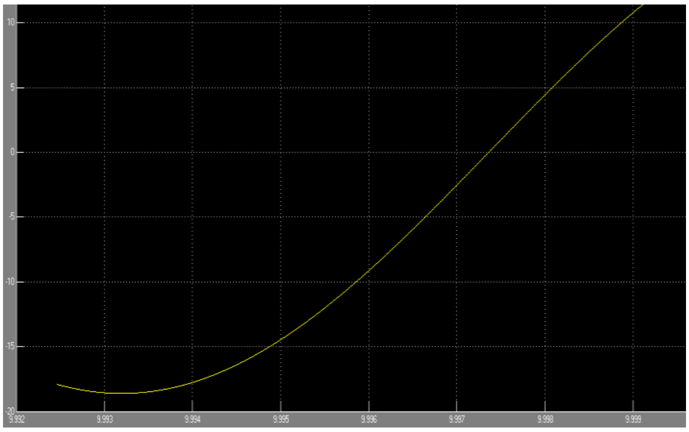

Fig. 16 experimental wave before installing upfc for radial system

B. After Installing UPFC

Experimental system shown in Fig. 8 is carried out as loop distribution system after installing UPFC. First, UPFC is used to achieve line loss minimum condition. Then, UPFC is used to regulate node 2 voltage to be equal in magnitude to the nominal voltage under line loss minimum condition. Finally, UPFC is used to regulate all node voltages to be within permissible voltage range, 200 ± 5%, under line loss minimum condition. In each case, the line currents, node voltages, and total line loss are measured and listed in Table II for comparison.

i) ***Line Loss Minimization**:* UPFC is installed in the loop system to achieve line loss minimum condition by controlling node 2 voltage to be as shown in (12). Table II shows the experimental results of all line currents, loop current *i*loop, all node voltages, UPFC series converter voltage *vc* , and total line loss. Fig. 9 shows the experimental waveforms of loop current, UPFC series converter voltage, reference and actual node 2 voltage in the *p–q* axes, reference and actual line 2 current in the *p–q* axes, reference and actual phase shift angle between the source and node 2 voltages, and rms line voltage of each node in the loop system before and after installing UPFC. Experimental results show that UPFC eliminates the loop current from loop system, and hence minimize the total line loss by 7.3%. However, the node 2 voltage is still less than the lower voltage limit.

ii) ***Node Voltage Equal in Magnitude to Nominal Source Voltage Under Loss Minimization:*** UPFC is installed in the loop system to regulate node 2 voltage to be equal in magnitude to the nominal source voltage (200 V) under line loss minimum condition by controlling node 2 voltage to be as shown in (18). Table II and Fig. 10 show the experimental results in the loop system before and after installing UPFC. Experimental results show that the UPFC regulates the node 2 voltage to be equal in magnitude to the nominal source voltage. However, the total line loss increases by 5.1%, and the node 1 voltage decreases and becomes less than the lower voltage limit.

iii) ***All Nodes Voltage Regulation under Loss Minimization to improve power quality:*** UPFC is installed in the loop system to achieve all node voltages to be within the permissible voltage limit under line loss minimum condition by controlling node 2 voltage to be as shown in (21). In this case, controlling the system to be under loss minimum condition is achieved by controlling node 2 voltage to be lag behind source voltage by the angle $\theta *$. Also, the reference magnitude of node 2 voltage is controlled in order to achieve all node voltages to be within the limit. Table II and Fig. 11 show the experimental results of loop system before and after installing UPFC. It is cleared that after installing UPFC, the reference and actual values agree well with each other. According to the control flow chart shown in Fig. 6, the UPFC starts with controlling node 2 voltage to achieve line loss minimization, and the estimated values have been used to check if the voltage at each node is within the permissible voltage limit or not. Fig. 12 shows the estimated and actual voltages of all nodes in case of controlling node 2 voltage to achieve line loss minimum condition. Since the estimated values of node 2 voltage, in case of loss minimization, is less than the lower voltage limit, the reference magnitude of node 2 voltage is changed to be equal to the nominal source voltage magnitude (200 V). In this case, estimated values have been used to check if node 1 and node 3 voltages are within the limit or not.

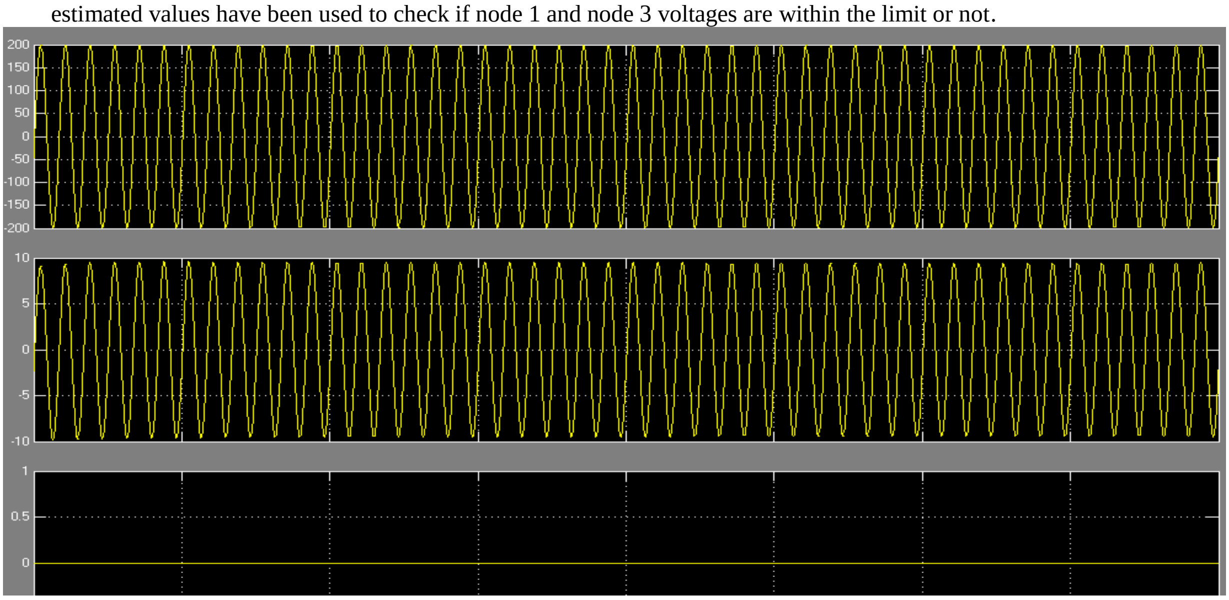

Fig. 17 experimental wave after installing upfc for loop system

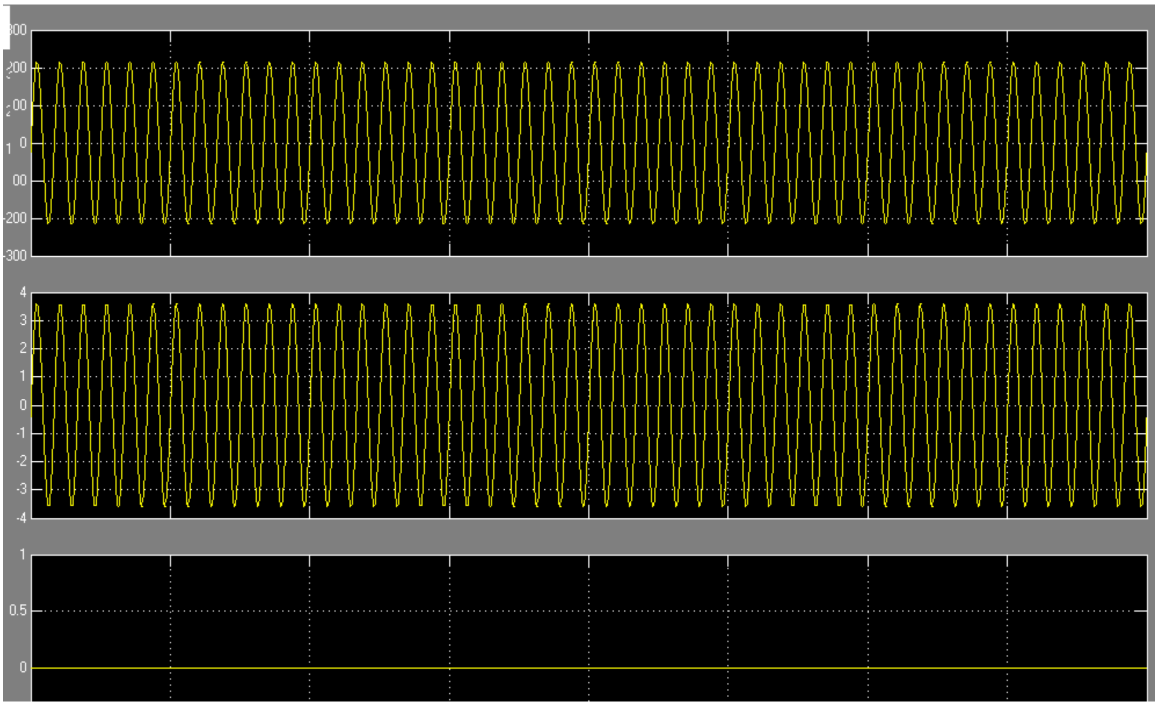

Fig. 18 experimental wave after installing upfc for radial system

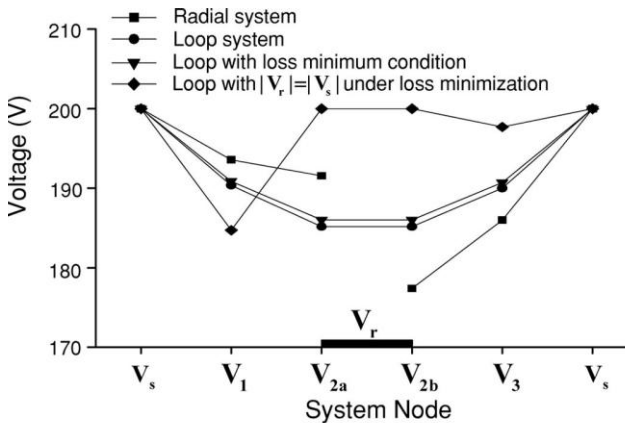

Fig. 19 Calculated node voltages before and after installing UPFC.

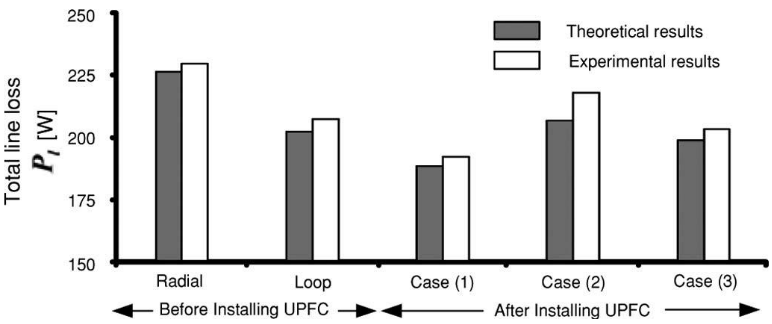

Fig.19 Total line loss.

Fig. 15 shows a comparison between theoretical and experimental results of total line loss in radial system, loop system without UPFC, and loop system with UPFC that is used to achieve line loss minimum condition, to achieve load voltage equal in magnitude to the nominal source voltage, and to achieve all node voltages to be within the permissible voltage limit under loss minimization. Also, Fig. 16 shows the rms line-to-line node voltages in each case. It is cleared that only in the last case, all node voltages are within the permissible voltage limit under loss minimization.

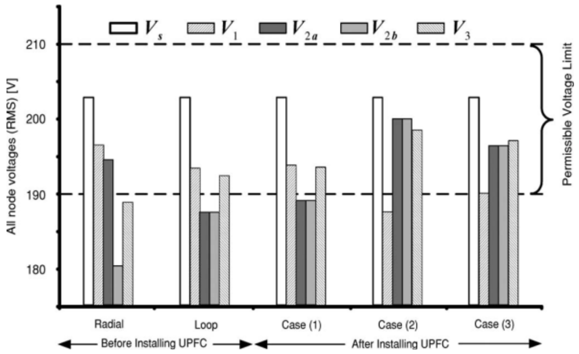

Fig. 20 RMS line-to-line node voltages.

VIII. CONCLUSION

This paper has presented the line loss minimum conditions and the control schemes of UPFC for the improvement of power quality. Regulating node voltage under line loss minimization has been achieved by controlling the phase angle of the controlled voltage. Installing UPFC to minimize the total line losses or to regulate the load voltage to be equal in magnitude to the nominal source voltage under loss minimization. Node voltage estimation has been proposed and the estimated voltages at each node agree well with their actual values. Experimental results prove that the UPFC has a great capability to regulate all node voltages to be with in the permissible voltage range under line loss minimum condition and it will improve the power quality in distribution system.

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