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A Model of A Differential Protection Relay

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Abstract—The analysis of a modelled differential protection relay is presented. The mathematical model was first developed from where diagrams were produced. A different approach in dealing with the instability problem caused by switching in-rush current in transformers - 'The voltage restraint method', is also presented. In this paper, a stability logic circuit was modelled to block the operation of the relay under "unreal fault" conditions. Tests and simulations show that the relay responds within 10 milliseconds; and an appreciable output was obtained at the differential current as low as 0.01Ampere while at the differential current of 0 Amp (no differential current) the relay was stable.

Keywords—Differential current, protection, restraining voltage, stability, current transformer.

I. INTRDUCTION

The differential relay's operation is based on the principles of Kirchoff's law which states that the sum of the currents in a node is zero. In the basic differential scheme, the currents in each phase are compared on the incoming and outgoing sides of the protected equipment. If they are not equal, the difference current is used to energize the operating coil of the relay. That implies that current transformers will be required at both sides of the equipment to facilitate the summation of currents as shown in fig 1.

II. MODELLING

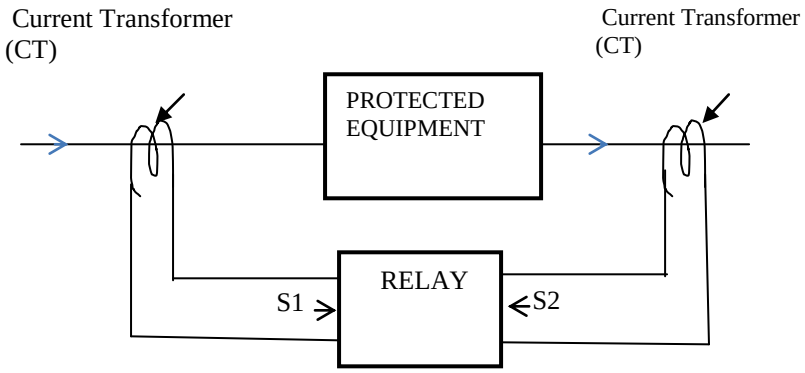


Fig.1.The basic differential protection

(1). Design Calculations

Let the inputs to the differential protection be $S_1$and S_2 such that

$$\left.\begin{aligned} S_1 &= K_{11} I_1 Z_1 \\ S_2 &= K_{21} I_2 Z_2 \end{aligned}\right\} \quad (1)$$

Where IZ = current converted to voltage
K_{11}; K_{21} = Conversion factors.

For stability, $\left|K_{11} I_1 Z_1\right| = \left|K_{21} I_2 Z_2\right|$ (2)

If $K_{11} = K_{21} = K$ and $I_1 = I_2 = I$, equation (2) now becomes

$$\left|KIZ_1\right| = \left|KIZ_2\right| \qquad (3)$$

Thus for stability Z_1 must be equal to Z_2, otherwise that could be condition of an uneven lengths of the current transformer (CT) pilots or/and unequal rated burdens of the input current transformers (CTs).
Now assuming in equation (3) $Z_n = K_a R_b$,
such that $Z_1 = K_3 R_1$ and $Z_2 = K_4 R_2$

$$\left|KK_3I_1Z_1\right| = \left|KK_4I_2Z_2\right| \qquad (4)$$

Where K3 and K_4 are factors
Applying the signals of eqn(4) into two different amplifiers with reference signals Sr_1 and Sr_2, the output expressions become:
$A_1(I_1K\,K_3R_1 - Sr_1)$ and $A_2\,(I_2K\,K_4\,R_2 - Sr_2\,)$
where $A_1$and A_2 are the amplifier gains.

Therefore $\left|A_1\left(KK_3I_1R_1 - Sr_1\right)\right| = \left|A_2\left(KK_4I_2R_2 - Sr_2\right)\right|$ (5)

If $A_1 = A_2 = A$; and $K_3 = K_4$ (Similar Circuits), then

$$\left|x\left(I_1R_1 - SR_1\right)\right| = \left|x\left(I_2R_2 - SR_2\right)\right| \qquad (6)$$

where $x = AK\,K_3 = A\,K\,K_4$
xI_1R_1-Sr_1 and xI_2R_2-Sr_2 are suppose to be equal but where they are not, they can be made equal by simply adjusting Sr_1 or Sr_2 .

The ports $\left|x\left(I_1R_1 - Sr_1\right)\right|$ and $\left|x\left(I_2R_2 - Sr_2\right)\right|$ are the complementary out-puts of the differential processor; while Sr_1 and Sr_2 can be called the "restraining signals".
By feeding the signals of equation (6) into a window comparator with gains B_1 and B_2, the final outputs of the differential circuit become;

$$\left|B_1x\left(I_1R_1 - Sr_1\right)\right| - \left|B_2x\left(I_2R_2 - Sr_2\right)\right|$$

and $$\left|B_2x\left(I_2R_2 - Sr_2\right)\right| - \left|x\left(I_1R_1 - Sr_1\right)\right| \qquad (7)$$

Again Since the circuits are identical
$B_1 = B_2 = B$, $Sr_1 = Sr_2$ and $R_1 = R_2 = R$
Hence eqn (7) can be reduced to:

$$C\left(I_1 - I_2\right)$$

$$C\left(I_2 - I_1\right) \qquad (8)$$

Where C = BxR

Equation (8) shows that the output of the differential circuit is dependent on the difference current, ΔI. When $I_1 = I_2$, the output is zero, signifying the stability condition for the differential circuit and $I_1 \neq I_2$ produces two complementary signals of the same magnitude but opposite polarities at the two output terminals of the processor.
The diagram representing eqns (1) to (8) is shown in figs 2.
When the model was initially simulated at various input current differentials it became apparent that some form of gain needed to be introduced in the window comparator to correspond to B_1 and B_2 in equation (7) so that the final output can correspond with the expressions, $C(I_1 - I_2)$ and $C(I_2 - I_1)$ eqn (8).

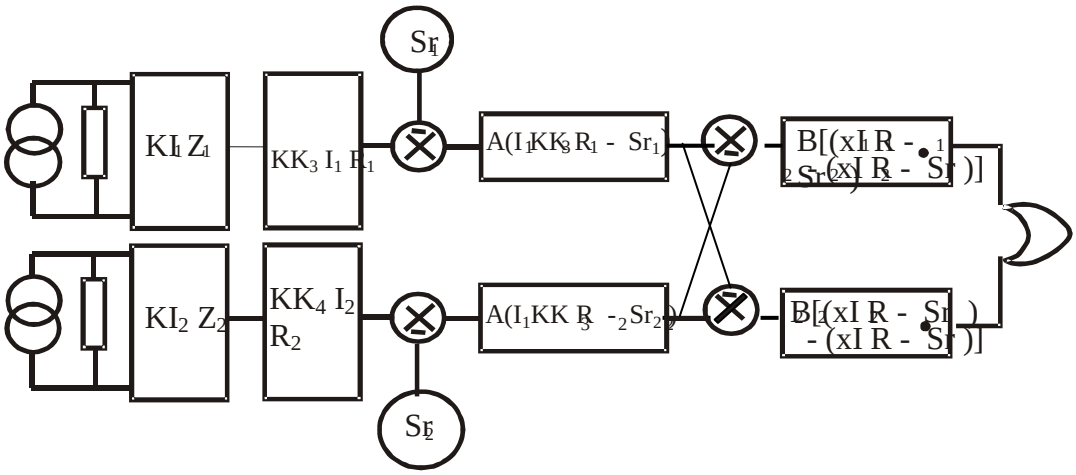


Fig 2. Block diagram of the model

III. PICK-UP SETTING

The basic differential current expressions are shown in eqns (1) to (8) but there could be need to determine the operating point of the scheme in order that it could be adaptable to various differential current conditions. This is achieved by feeding the positive part of the compliment ary signals of eqn.(8) into another amplifier circuit with variable initial condition, Vp. So that the final differential output becomes

$$[C(I_1 - I_2) \text{ OR } C(I_2 - I_1)]\text{-Vp} \qquad (9)$$

Where Vp is the pick-up setting of the differential circuit.

IV. INSTABILITY

(1). Mismatch In Current Transformers

In the new relay, no external circuit is required to remedy mismatch in current transformers. It has special facility for CT mismatch through the feed back resistors, R_{11} and R_{21} in the current-to-voltage converter. A rheostat or a bank of selectable resistors are used to balance the mismatch in CTs and also at the condition of uneven lengths of the CT pilots.

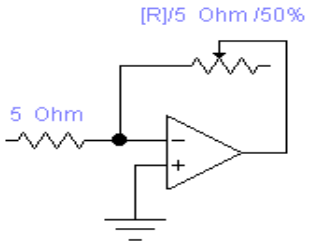


Fig3 Adjusting R11orR21 to remedy CT match

(2). Switching - in Inrush current

During switching-on of a transformer, the inrush current generates harmonics on only the side of the transformer that is switched on. This can offset the stability of the differential scheme. In conventional differential schemes, tuned circuits are used to block the resulting transient signals (harmonics) but this model uses the voltage restraining technique. It is a well-known fact that during short circuit, the voltage deepens and current rises. Therefore during fault it is expected that the voltage will drop and current rises. So during switching-on of a transformer this new model declares the condition where up to 72% of the supply voltage is available as a no crises situation and allows tripping when less than 72% of the supply voltage is available. After 10mseconds, when the transient might have died, the timer switches of the restraining circuit and the normal differential operation remains. The voltage restraint occurs only during the switching-on period. The minimum voltage for stability, Vs, based on VT ratio of X/110, can be expressed as;

$$\text{Vs}= \frac{C}{20\pi} h\int_0^{\pi} Sin\theta\partial\theta \qquad (10)$$

Where c = 0.72 (72%)

h= conversion factor

The circuit to realize this is shown in fig 4.

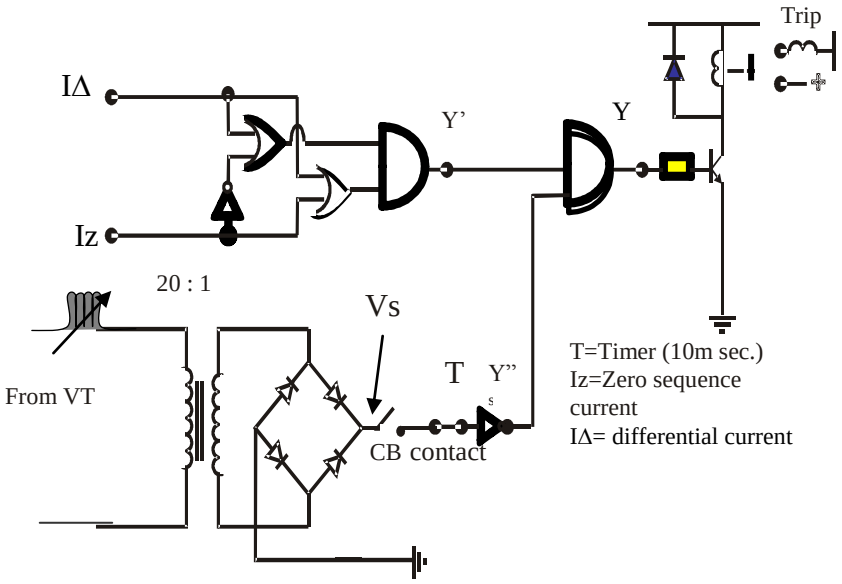


Fig 4: Stability logic circuit

Table1. Truth table for stability logic (fig4)

	IΔ	Iz	Vs	Y'	Y"	Y
1	0	0	0	0	1	0
2	0	0	1	0	0	0
3	0	1	0	0	1	0
4	0	1	1	0	0	0
5	0	0	1	1	1	1
6	1	0	1	1	0	0
7	1	1	0	1	1	1
8	1	1	1	1	0	0

If the VT in-put in fig.4. is 110V (when VT ratio is X/110), equation (10) yields 2.52 volts at full voltage and unity h. This voltage is fed into a TTL logic whose 'high' definition is 2.50V. The truth table of fig4 is shown in table1. From Table1, it can be seen that it is only during conditions 5 and 7 the differential scheme will operate; and these are conditions when there are "real faults". Conditions 6 and 8 suggest unreal fault conditions. It is very clear that condition 6 indicates magnetizing inrush current since there was restraining voltage. Condition 8 suggests that there were both magnetizing inrush current and emergence of zero sequence component of current. This new model discriminates correctly since there were no operations in these conditions. The minimum voltage to ensure stability of the new scheme is shown in table2 based on 72% voltage restraint.

Table2. Minimum voltage for stability at 72% voltage restraint.

Primary Voltage (KV)	Minimum for stability (KV)
11	7.92
33	23.76
132	95.04
330	237.6

These minimum stability voltages can still be adjusted at the desecrations of the protection engineer.

V. TESTS AND SIMULATIONS

Various modules of the new protection relay, including the processor at various differential conditions, were simulated and the results are shown below:

(1). Thecurrent-to-Voltage Converter:

The function of this device is to convert the input current, from the current transformer, to voltage which is then applied to the processor. The output of this device, when R11/ 21 were varied, is shown in fig5.

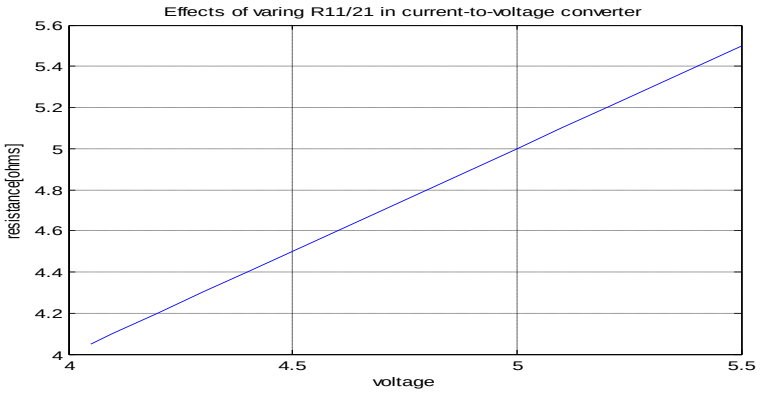
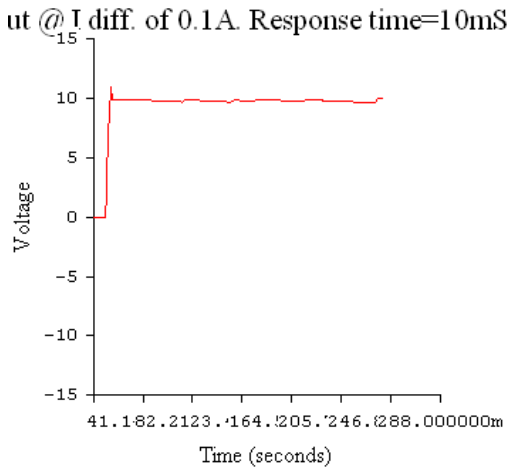


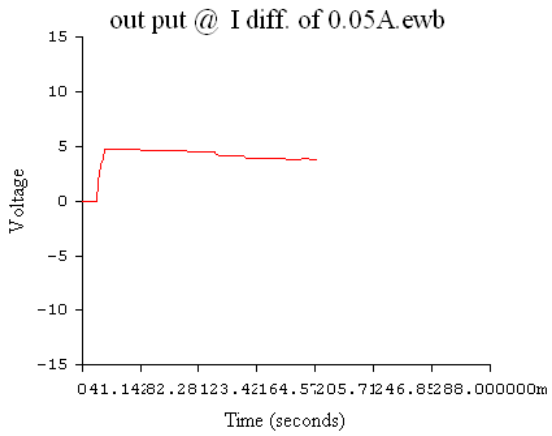
Fig5: Effect of varying R11 / R21 in the current-to-voltage converter

(2). The Processor:

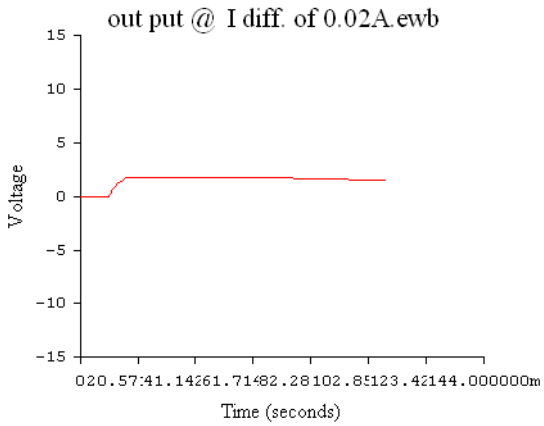
The performance of the processor was simulated at various differential current conditions. The results are shown in fig.6 (a to f). For differential Current of O.1 Amp, that is, one source was supplying 1 Amp. while the other was supplying 1.1 Amps. The output voltage was 10.0V as can be seen in Fig6 (a). At the differential currents of 0.05A and 0.02A; the output voltages were 5.0V and 2.0 V respectively. These are displayed as Fig.6 (b) and (c) respectively. Fig.6(d) displays the output at the differential current of 0.01 Amp. The output at the differential current of 0.0, that is, no differential current, is zero as can be seen very clearly in fig.6(e). Fig. 6(d) shows the



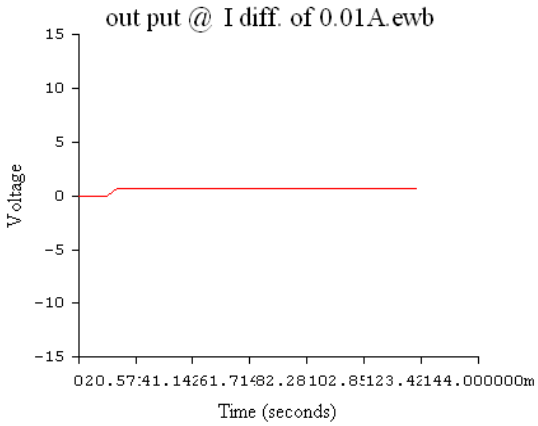
(a)



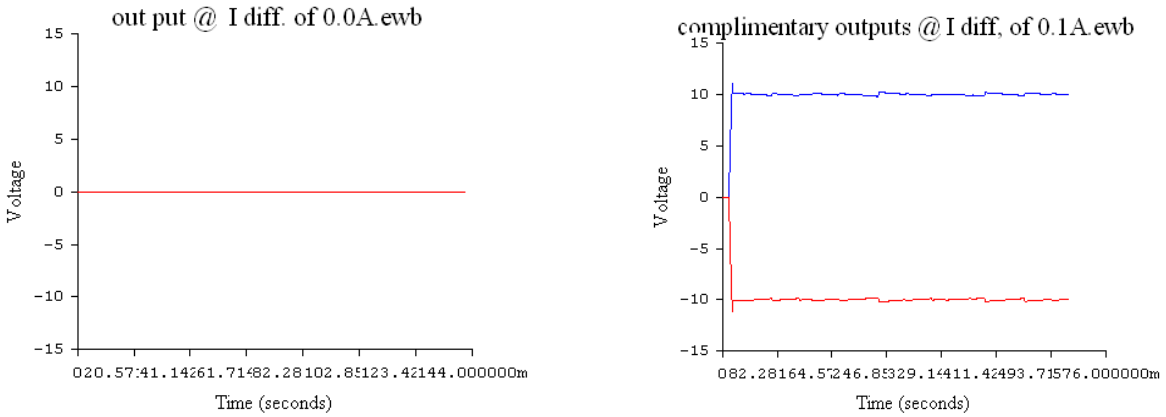
(b)



(c)



(d)



(e) (f)

Fig. 6.The responses at various differential current values.

(a) output at differential current of 0.1A
(b) output at differential current of 0.05A
(c) output at differential current of 0.02A
(d) output at differential current of 0.01A
(e) output at differential current of 0A
(f) complimentary outputs of the processor

complimentary outputs of the processor at the differential current of 0.1A. . These outputs show that the response of the new differential relay is very reliable. The response time was 10mSeconds (one twentieth of a power cycle of 50Hz). Fig.7 shows the characteristic of the model.

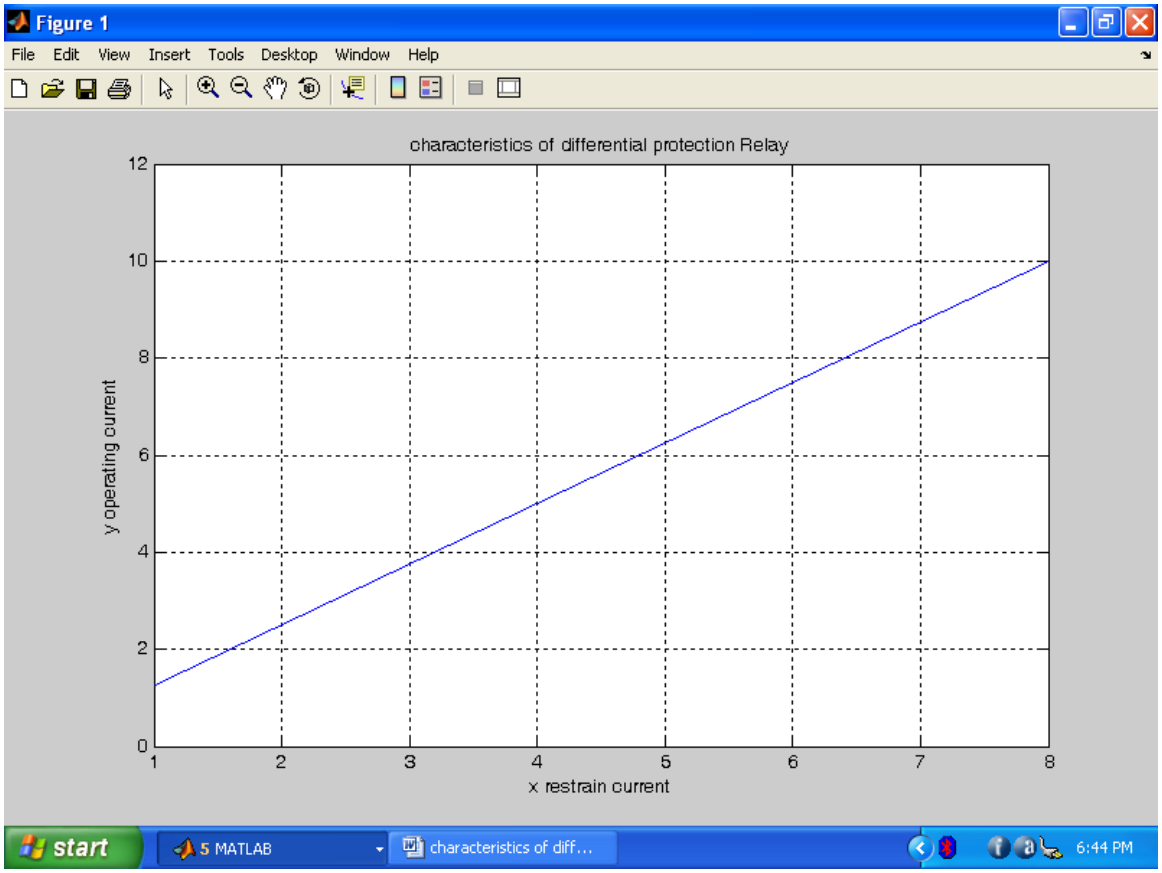


Fig7: The characteristic of the model

VI. CONCLUSION

The modelled new differential protection relay is presented. The model introduces new method of dealing with the instability problem caused by switching in-rush current usually associated with transformers. A stability logic is modelled to ensure that the relay 0perates only on real faults. The use of variable resistors at the current-to- voltage converter provides

remedy for mismatch in input current transformers. The results of the tests and simulations show that the designed model can work.

REFERENCES

[1]. Mason CR. "The art and science of protective relays". John Willy and sons inc.1956.

[2]. Andrichak J G, Cardinas J. "Bus differential protection". 22nd Western Protective relay Conference, Spoken Washington 24th Oct. 1995

[3]. Horowitz SH, Phadke AG. "Power System relaying". Research studies press LTD 1995.

[4]. BBC. "BBC protects your high voltage plants". BBC Brown Boveri coy Baden.

[5]. Electricity Council." Power system protection". Peter Peregrinus LTD London 1981.

[6]. Ezechukwu OA. :Solid state phase comparator for power system protection". NIEEE ICEPT Proc. Oct. 2007

[7]. GEC-"Protective relay application guide". GEC measurements PLC London 1987.

[8]. MELCO. "Bus protection relay system maintainance/operating manual"SE103B,Mitsubishi Elect. Coy 1978

[9]. Ram B, Vishwakarma DN." Power system protection and switchgear". Tata Mc grawHill new Delhi 1995.

[10]. Rushton J. "The fundamental characteristics of pilot wire differential system". PNC 1961 vol 1084

[11]. Siemens coy. "Transformer differential protective relay system" operating/maintenance instruction MWBR T22-10/10

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