International Journal of Engineering Research and Development
***e**-ISSN: 2278-067X, **p**-ISSN: 2278-800X, www.ijerd.com*
Volume 3, Issue 5 (August 2012), PP. 47-55

Compensation for Voltage and Current in Multifeeder System Using MC-UPQC

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Abstract*—This paper presents a new unified power-quality conditioning system (MC-UPQC), capable of simultaneous compensation for voltage and current in multibus/multifeeder systems. In this configuration, one shunt voltage-source converter (shunt VSC) and two or more series VSCs exist. The system can be applied to adjacent feeders to compensate for supply-voltage and load current imperfections on the main feeder and full compensation of supply voltage imperfections on the other feeders. In the proposed configuration, all converters are connected back to back on the dc side and share a common dc-link capacitor. Therefore, power can be transferred from one feeder to adjacent feeders to compensate for sag/swell and interruption. The performance of the proposed configuration has been verified through simulation studies using MATLAB/SIMULATION on a two-bus/two-feeder system show the effectiveness of the proposed configuration.

***Index Terms*—Power quality (PQ), MATLAB/SIMULATION, unified power-quality conditioner (UPQC), voltage source converter (VSC), MultiConverter Unified Power Quality Conditioner (MC-UPQC)**

I. INTRODUCTION

Power quality is the combination of voltage quality and current quality. Voltage quality is concerned with the deviation of actual voltage from ideal voltage. Current quality is the equivalent definition for the current. Any deviation of voltage or current from the ideal is a power quality disturbance. Any change in the current gives a change in the voltage and the other way around. Voltage disturbance originate in the power network and potentially affect the customers, where as current disturbance originate with customer and potentially affect the network [1].

As commercial and industrial customers become more and more reliant on high quality and high-reliability electric power, utilities have considered approaches that would provide different options or levels of premium power for those customers who require something more than what the bulk power system can provide insufficient power quality can be caused by failures and switching operations in the network, which mainly result in voltage dips, interruptions, and transients and network disturbances from loads that mainly result in flicker (fast voltage variations), harmonics, and phase imbalance.

Momentary voltage sags and interruptions are by far the most common disturbances that adversely impact electric customer process operations in large distribution systems. In fact, an event lasting less than one-sixtieth of a second (one cycle) can cause a multimillion-dollar process disruption for a single industrial customer. Several compensation [3] devices are available to mitigate the impacts of momentary voltage sags and interruptions. When PQ problems are arising from nonlinear customer loads, such as arc furnaces, welding operations, voltage flicker and harmonic problems can affect the entire distribution feeder [2]. Several devices have been designed to minimize or reduce the impact of these variations.

The primary concept is to provide dynamic capacitance and reactance to stabilize the power system. This is typically accomplished by using static switching devices to control the capacitance and reactance, or by using an injection transformer to supply the reactive power to the system. Now a days, voltage based converter improving the power quality (PQ) of power distribution systems.

A Unified Power Quality Conditioner (UPQC)[4] can perform the functions of both D-STATCOM and DVR. The UPQC consists of two voltage source converters (VSCs) that are connected to a common dc bus. One of the VSCs is connected in series with a distribution feeder, while the other one is connected in shunt with the same feeder. The dc-links of both VSCs are supplied through a common dc capacitor. It is also possible to connect two VSCs to two different feeders in a distribution system is called Interline Unified Power Quality Conditioner (IUPQC)

This paper presents a new Unified Power Quality Conditioning system called MultiConverter Unified Power Quality Conditioner (MC-UPQC) [5].

II. CIRCUIT CONFIGURATION

As shown in this Fig.1 two feeders connected to two different substations supply the loads L1 and L2. The MC-UPQC is connected to two buses BUS1 and BUS2 with voltages of ut1 and ut2, respectively. The shunt part of the MC-UPQC is also connected to load L1 with a current of il1.

Supply voltages are denoted by us1 and us2 while load voltages are ul1 and ul2. Finally, feeder currents are denoted by is1 and is2 and load currents are il1 and il2.

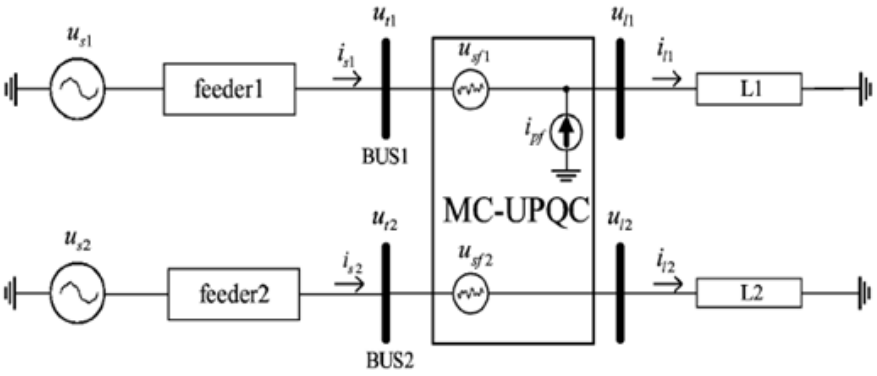

Fig. 1 Single - line diagram of MC-UPQC connected distribution system

Bus voltages ut1 and ut2 are distorted and may be subjected to sag/swell. The load L1 is a nonlinear/sensitive load which needs a pure sinusoidal voltage for proper operation while its current is non-sinusoidal and contains harmonics. The load L2 is a sensitive/critical load which needs a purely sinusoidal voltage and must be fully protected against distortion, sag/swell and interruption. These types of loads primarily include production industries and critical service providers, such as medical centers, airports, or broadcasting centers where voltage interruption can result in severe economical losses or human damages

III. MC–UPQC STRUCTURE

The internal structure of the MC–UPQC is shown in Fig.2. It consists of three VSCs (VSC1, VSC2, and VSC3) which are connected back to back through a common dc-link capacitor. In the proposed configuration, VSC1 is connected in series with BUS1 and VSC2 is connected in parallel with load L1 at the end of Feeder1. VSC3 is connected in series with BUS2 at the Feeder2 end.

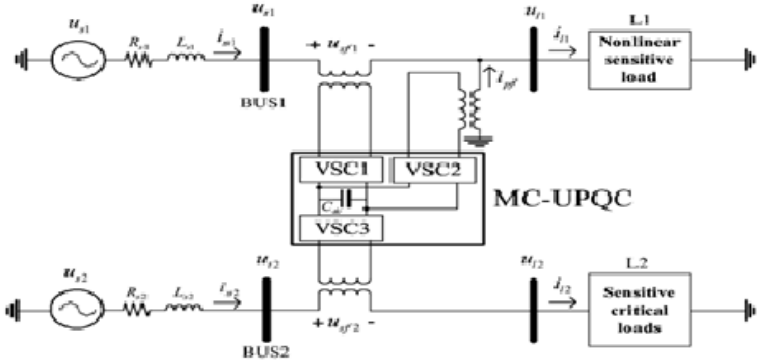

Fig. 2 Typical MC-UPQC used in a distribution system.

Reactor and high-pass output filter as shown in Fig .3. The commutation reactor (Lf) and high- pass output filter (R f, C f) are connected to prevent the flow of switching harmonics into the power supply. Each of the three VSCs in Fig. 2 is realized by a three-phase converter with a commutation

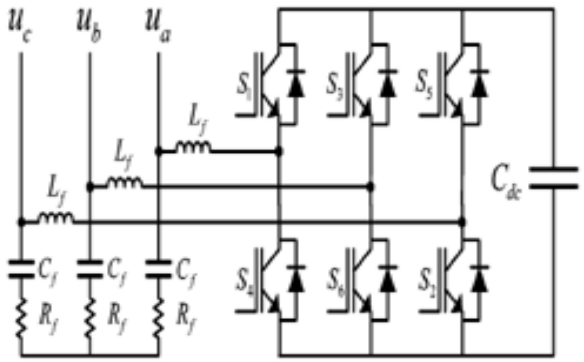

Fig.3 Schematic structure of a VSC

As shown in Fig. 2, all converters are supplied from a common dc-link capacitor and connected to the distribution system through a transformer. Secondary (distribution) sides of the series-connected transformers are directly connected in series with BUS1 and BUS2, and the secondary (distribution) side of the shunt-connected transformer is connected in parallel with load L1. The aims of the MCUPQC are:

1) To regulate the load voltage (ul1) against sag/swell, interruption, and disturbances in the system to protect the Non-Linear/sensitive load L1.
2) To regulate the load voltage (ul2) against sag/swell, interruption, and disturbances in the system to protect the sensitive/critical load L2.
3) To compensate for the reactive and harmonic components of nonlinear load current (il1)

In order to achieve these goals, series VSCs (i.e., VSC1 and VSC3) operate as voltage controllers while the shunt VSC (i.e., VSC2) operates as a current controller

IV. CONTROL STRATEGY

As shown in Fig. 2, the MC-UPQC consists of two series VSCs and one shunt VSC [6]-[8] which are controlled independently. The switching control strategy for series VSCs and the shunt VSC are selected to be sinusoidal pulse width-modulation (SPWM) voltage control and hysteresis current control, respectively. Details of the control algorithm, which are based on the d-q method [12], will be discussed later.

Shunt-VSC: Functions of the shunt-VSC are:

1) To compensate for the reactive component of load L1 current;
2) To compensate for the harmonic components of load L1 current;
3) To regulate the voltage of the common dc-link capacitor.

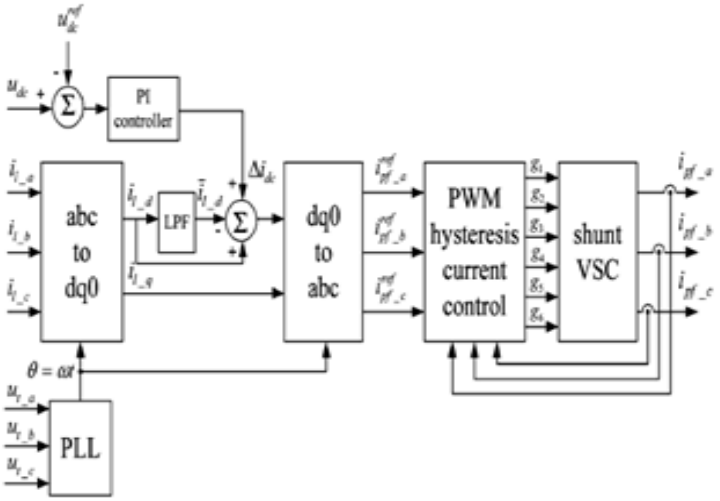

Fig.4 Control block diagram of the shunt VSC.

Fig.4 shows the control block diagram for the shunt VSC. The measured load current (il-abc) is transformed into the synchronous dqo reference frame by using

$$i_{l\_dq0} = T_{abc}^{dq0}\, i_{l\_abc} \qquad (1)$$

Where the transformation matrix is shown in (2),

$$T_{abc}^{dq0} = 2/3 \begin{pmatrix} \cos(\omega t) & \cos(\omega t\text{-}120^\circ) & \cos(\omega t\text{+}120^\circ) \\ -\sin(\omega t) & -\sin(\omega t\text{-}120^\circ) & -\sin(\omega t\text{+}120^\circ) \\ 1/2 & 1/2 & 1/2 \end{pmatrix} \qquad (2)$$

By this transform, the fundamental positive-sequence component, which is transformed into dc quantities in the axes, can be easily extracted by low-pass filters (LPFs). Also, all harmonic components are transformed into ac quantities with a fundamental frequency shift

$$i_{l\text{-}d} = i_{l\_d} + i_{l\_d} \qquad (3)$$

$$i_{l\_q} = i_{l\_q} + i_{l\_q} \qquad (4)$$

Where $i_{l\text{-}d}$ and $i_{l\text{-}q}$ are d-q components of load current, i_{l_d} and i_{l_q} are dc components, and il_d and i_{l_q} are the ac components of $i_{l\text{-}d,}$ and $i_{l\text{-}q.}$

If i_s is the feeder current and i_{pf} is the shunt VSC current and knowing $i_s = i_l - i_{pf}$, then d–q components of the shunt VSC reference current are defined as follows

$$i_{pf\_d}^{ref} = i_{l\_d} \quad (5)$$

$$i_{pf\_q}^{ref} = i_{l\_q} \quad (6)$$

Consequently, the d–q components of the feeder current are

$$i_{s\_d} = i_{l\_d} \quad (7)$$

$$i_{s\_q} = 0. \quad (8)$$

This means that there are no harmonic and reactive components in the feeder current. Switching losses cause the dc-link capacitor voltage to decrease. Other disturbances, such as the sudden variation of load, can also affect the dc link. In order to regulate the dc-link capacitor voltage, a proportional–integral (PI) controller is used as shown in Fig. 4. The input of the PI controller is the error between the actual capacitor voltage (u_{dc}) and its reference value (u_{dc}^{ref}).
The output of the PI controller (i.e., delta i_{dc}) is added to the component of the shunt-VSC reference current to form a new reference current as follows:

$$\begin{cases} i_{pf\_d}^{ref} = i_{l\_d} + \Delta i_{dc} \\ i_{pf\_q}^{ref} = i_{l\_q} \end{cases} \quad (9)$$

As shown in Fig. 4, the reference current in (6.11) is then transformed back into the *abc* reference frame. By using PWM hysteresis current control, the output-compensating currents in each phase are obtained.

$$i_{pf\_abc}^{ref} = T_{dq0}^{abc}\, i_{pf\_dq0}^{ref};\ (T_{dq0}^{abc} = T_{abc}dq0^{-1}) \quad (10)$$

Series-VSC: Functions of the series VSCs in each feeder are:
1 To mitigate voltage sag and swell;
2 To compensate for voltage distortions, such as harmonics;
3 To compensate for interruptions (in Feeder2 only).

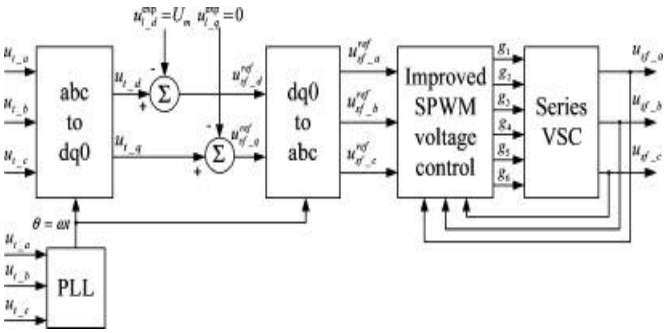

Fig.5 *Control block diagram of the series VSC.*

The control block diagram of series VSC is shown in Fig.5.The bus voltage ($u_{t\text{-}abc}$) is detected and then transformed into the synchronous dq0 reference frame using

$$u_{t\_dq0} = T_{abc}^{dq0}\, u_{t\_abc} = u_{t1p} + u_{t1n} + u_{th} \quad (11)$$

Where

$$\begin{cases} u_{t1p} = [u_{t1p\_d} \quad u_{t1p\_q} \quad 0]^T \\ u_{t1n} = [u_{t1n\_d} \quad u_{t1n\_q} \quad 0]^T \\ u_{t10} = [0 \ 0 \ u_{00}]^T \\ u_{th} = [u_{th\_d} \quad u_{th\_q} \quad u_{th\_0}]^T \end{cases} \quad (12)$$

u_{t1p}, u_{t1n} and u_{t10} are fundamental frequency positive-, negative-, and zero-sequence components, respectively, and u_{th} is the harmonic component of the bus voltage.

According to control objectives of the MC-UPQC, the load voltage should be kept sinusoidal with constant amplitude even if the bus voltage is disturbed. Therefore, the expected load voltage in the synchronous dqo reference frame ($u^{exp}_{l\text{-}dqo}$) only has one value

$$u_{l\_dq0}^{exp} = T_{abc}^{dq0}\, u_{l\_abc}^{exp} = \begin{pmatrix} U_m \\ 0 \\ 0 \end{pmatrix} \qquad (13)$$

Where the load voltage in the *abc* reference frame ($u_{exp\ l\text{-}abc}$) is

$$u_{l\_dq0}^{exp} = \begin{pmatrix} U_m \cos(\omega t) \\ U_m \cos(\omega t\text{-}120^\circ) \\ U_m \cos(\omega t+120^\circ) \end{pmatrix} \qquad (14)$$

The compensating reference voltage in the synchronous dqo reference frame ($u^{exp}_{l\text{-}dqo}$) is defined as

$$u_{sf\_dq0}^{ref} = u_{t\_dq0} - u_{l\_dq0}^{exp} \qquad (15)$$

This means $u_{t1p\text{-}d}$ in (12) should be maintained at U_m while all other unwanted components must be eliminated. The compensating reference voltage in (15) is then transformed back into the abc reference frame. By using an improved SPWM voltage control technique (sine PWM control with minor loop feedback)[8], the output compensation voltage of the series VSC can be obtained

V. SIMULATION RESULTS

The proposed MC-UPQC and its control schemes have been tested through extensive case study simulations using MATLAB/SIMULATION. In this section, simulation results are presented, and the performance of the proposed MC-UPQC system is shown.

A. Distortion and Sag/Swell on the Bus Voltage

Let us consider that the power system in Fig. 2 consists of two three-phase three-wire 380(v) (rms, L-L), 50-Hz utilities. The BUS1 voltage (u_{t1}) contains the seventh-order harmonic with a value of 22%, and the BUS2 voltage(u_{t2})contains the fifth order harmonic with a value of 35%. The BUS1 voltage contains 25% sag between 0.1s<t<0.2s and 20% swell between0.2s<t<0.3s. The BUS2 voltage contains 35% sag between 0.25s<t<0.3s and 30% swell between 0.3s.The nonlinear/sensitive load L1 is a three-phase rectifier Load which supplies an RL load of 10Ω and 3 ʅH. Finally, the critical load L2 contains a balanced RL load of 10Ω and 100mH.

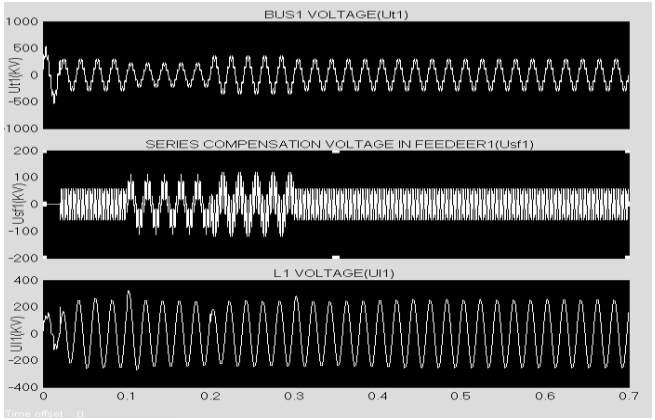

Fig.8 BUS1 voltage, series compensating voltage, and load voltage in Feeder1.

The MC–UPQC is switched on at t=0.02 s. The BUS1 voltage, the corresponding compensation voltage injected by VSC1, and finally load L1 voltage are shown in Fig.8

In all figures, only the phase a waveform is shown for simplicity. Similarly, the BUS2 voltage, the corresponding compensation voltage injected by VSC3, and finally, the load L2 voltage are shown in Fig.9

As shown in these figures, distorted voltages of BUS1 and BUS2 are satisfactorily compensated for across the loads L1 and L2 with very good dynamic response.

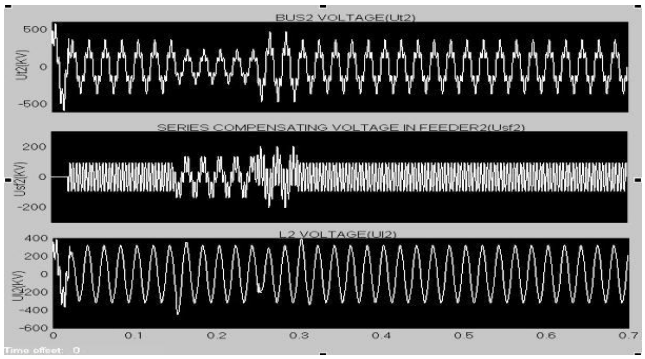

Fig.9 *BUS2 voltage, series compensating voltage, and load voltage in Feeder2.*

The nonlinear load current, its corresponding compensation current injected by VSC2, compensated

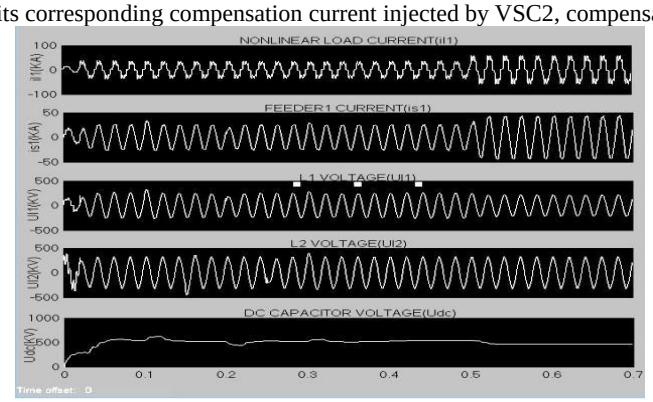

Fig.10 *Nonlinear load current, compensating current, Feeder1 current and capacitor voltage.*

Finally, the dc-link capacitor voltage are shown in Fig.10 Feeder1 current, and, the distorted nonlinear load current is compensated very well, and the total harmonic distortion (THD) of the feeder current is reduced from 26.6% to less than 5% as shown in fig.11 Also, the dc voltage regulation loop has functioned properly under all disturbances, such as sag/swell in both feeders

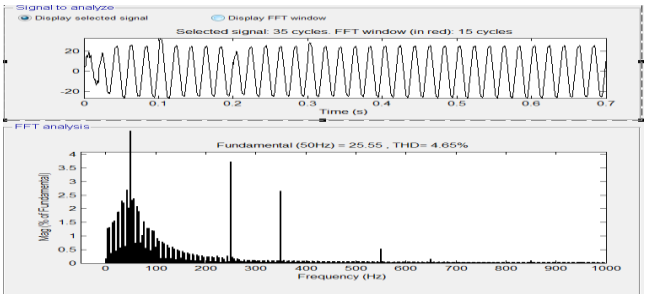

Fig.11 total hormonic distortion of feeder current

B. Upstream Fault on Feeder2

When a fault occurs in Feeder2 (in any form of L-G, L-L-G, and L-L-L-G faults), the voltage across the sensitive/critical load L2 is involved in sag/swell or interruption. This voltage imperfection can be compensated for by VSC2. In this case, the power required by load L2 is supplied through VSC2 and VSC3. This implies that the power semiconductor switches of VSC2 and VSC3 must be rated such that total power transfer is possible. This may increase the cost of the device, but the benefit that may be obtained can offset the expense. In the proposed configuration, the sensitive/critical load on Feeder2 is fully protected against distortion, sag/swell, and interruption. Furthermore, the regulated voltage across the sensitive load on Feeder1 can supply several customers who are also protected against distortion, sag/swell, and momentary interruption. Therefore, the cost of the MC-UPQC must be balanced against the cost of interruption, based on reliability indices, such as the customer average interruption duration index (CAIDI) and customer average interruption frequency index(CAIFI).

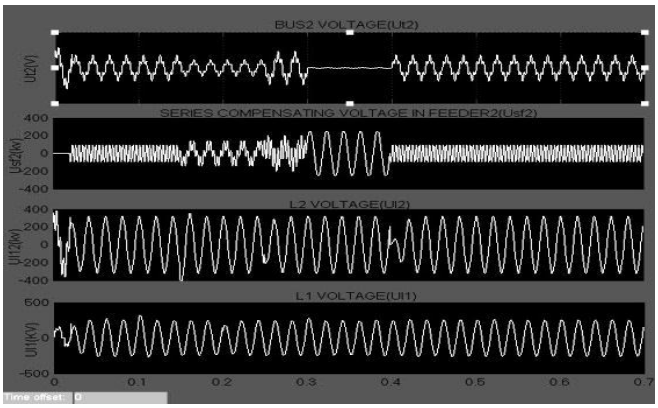

Fig.12 Simulation results for an upstream fault on Feeder2: BUS2 voltage, compensating voltage, and loads L1 and L2 voltages.

It is expected that the MC-UPQC cost can be recovered in a few years by charging higher tariffs for the protected lines. The performance of the MC-UPQC under a fault condition on Feeder2 is tested by applying a three-phase fault to ground on Feeder2 between 0.3s<t<0.4 s. Simulation results are shown in Fig.12

C. Load Change

To evaluate the system behavior during a load change, the nonlinear load L1 is doubled by reducing its resistance to half at t=0.5 s. The other load, however, is kept unchanged. The system response is shown in Fig.13

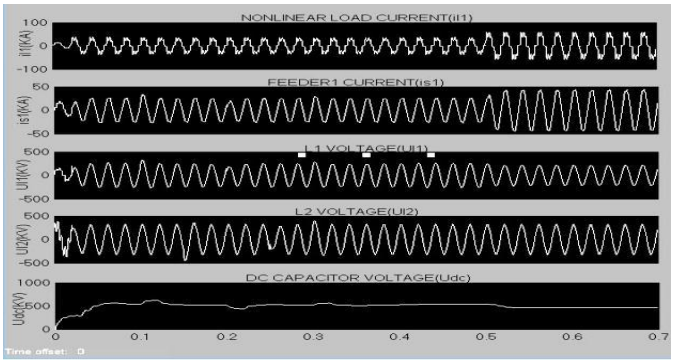

Fig.13 Simulation results for load change: nonlinear load current, Feeder1 current, load L1 voltage, load L2 voltage, and dc-link capacitor voltage.

It can be seen that as load L1 changes, the load voltages (U_{l1} and U_{l2}) remain undisturbed, the dc bus voltage is regulated, and the nonlinear load current is compensated.

D. Unbalance Voltage

The control strategies for shunt and series VSCs, which are introduced in Section II, are based on the d–q method. They are capable of compensating for the unbalanced source voltage and unbalanced load current. To evaluate the control system capability for unbalanced voltage compensation, a new simulation is performed. In this new simulation, the BUS2 voltage and the harmonic components of BUS1 voltage are similar to those given in Section IV. However, the fundamental component of the BUS1 voltage ($U_{t1fundamental}$) is an unbalanced three-phase voltage with an unbalance factor (U_- /U_+) of 40%. This unbalance voltage is given by

$$U_{t1fundamental} = \begin{bmatrix} 0.31\cos(\omega t+46^\circ) \\ 0.31\cos(\omega t-106^\circ) \\ 0.155\cos(\omega t+210^\circ) \end{bmatrix} \qquad (16)$$

The simulation results for the three-phase BUS1 voltage series compensation voltage, and load voltage in feeder 1 are shown in Fig. 14

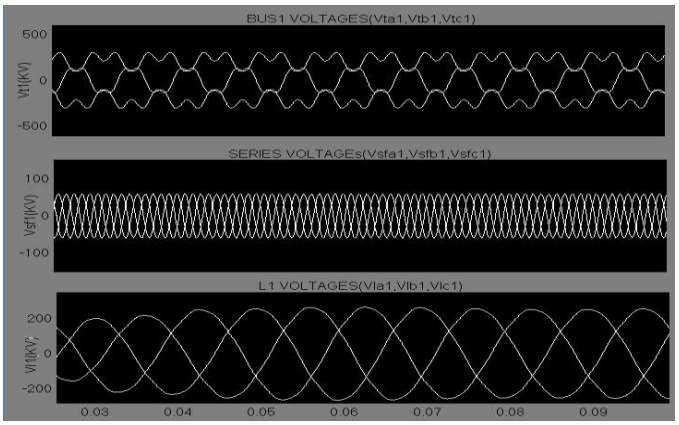

Fig.14 BUS1 voltage, series compensating voltage, and load voltage in Feeder1 under unbalanced source voltage.

The simulation results show that the harmonic components and unbalance of BUS1 voltage are compensated for by injecting the proper series voltage. In this figure, the load voltage is a three-phase sinusoidal balance voltage with regulated amplitude.

VI. CONCLUSION

The present topology illustrates the operation and control of Multi Converter Unified Power Quality Conditioner (MC-UPQC). The system is extended by adding a series VSC in an adjacent feeder. The device is connected between two or more feeders coming from different substations. A non-linear/sensitive load L-1 is supplied by Feeder-1 while a sensitive/critical load L-2 is supplied through Feeder-2. The performance of the MC-UPQC has been evaluated under various disturbance conditions such as voltage sag/swell in either feeder, fault and load change in one of the feeders. In case of voltage sag, the phase angle of the bus voltage in which the shunt VSC (VSC2) is connected plays an important role as it gives the measure of the real power required by the load. The IUPQC can mitigate voltage sag in Feeder-1 and in Feeder-2 for long duration.Compared to a conventional UPQC, the proposed topology is capable of fully protecting critical and sensitive loads against distortions, sags/swell, and interruption in two-feeder systems. The idea can be theoretically extended to multibus/multifeeder systems by adding more series VSCs. The performance of the MC-UPQC is evaluated under various disturbance conditions and it is shown that the proposed MC-UPQC offers the following advantages:

1. Power transfer between two adjacent feeders for sag/swell and interruption compensation;
2. Compensation for interruptions without the need for a battery storage system and, consequently, without storage capacity limitation;
3. Sharing power compensation capabilities between two adjacent feeders which are not connected.

From above discussion, it has been observed that an MC-UPQC is able to protect the distribution system from various disturbances occurring either in Feeder-1 or in Feeder-2. As far as the common dc link voltage is at the reasonable level, the device works satisfactorily. The angle controller ensures that the real power is drawn from Feeder-1 to hold the dc link voltage constant.

Therefore, even for voltage sag or a fault in Feeder-2, VSC-2 passes real power through the dc capacitor onto VSC-1 and VSC-3 to regulate the voltage U_{l1} and U_{l2} .Finally when a fault occurs in Feeder-2 or Feeder-2 is lost, the power required by the Load L-2 is supplied through both the VSCs(VSC2 and VSC3). This implies that the power semiconductor switches of the VSCs must be rated such that the total power transfer through them must be possible. This may increase the cost of this device. However, the benefit that may be obtained can offset the expense.

In the MC-UPQC configuration, the sensitive load is fully protected against sag/swell and interruption. The sensitive load is usually a part of a process industry where interruptions result in severe economic loss. Therefore, the cost of the series part of MC-UPQC must be balanced against cost of interruptions. It is expected that a part of MC-UPQC cost can be recovered in 5–10 years by charging higher tariff for the protected line. Furthermore, the regulated bus can supply several customers who are also protected against sag and swell.

The remaining part of the MC-UPQC cost can be recovered by charging higher tariff to this class of customers. Such detailed analysis is required for each IUPQC installation. In conclusion, the performance under some of the major concerns of both customer and utility e.g., harmonic contents in loads, unbalanced loads, supply voltage distortion, system disturbances such as voltage sag, and fhas been studied. The MC-UPQC has been shown to compensate for several of these events successfully.

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