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Design and Analysis of Multirate Filter for Wimax Application

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Abstract:- Design of programmable multirate filters has been proposed which can be used in digital transceivers that meets 802.16d/e (Wimax) standard in wireless communication. The wide spread use of digital representation of signals for transmission and storage has created challenges in area of digital signal processing [1]. Design is based on idea of software radio tech. and theorem of multirate signal processing the proposed design can be implemented on FPGA and can easily replace tradionally ASICs. The filters are designed using the powerful FDA (filter design and analysis) tool in MATLAB.

Keywords:- Duc,Ddc,Wimax, Sdr, Fda,Fpga.

I. INTRODUCTION

From the last few years telecom technology has gained wide popularity around the world mainly due to huge usage of cellular phones and wireless devices[2]. SDR is a wireless interface tech. that provides compatibility between different communication standards so that they can be implemented into a single transceiver. Software defined radio (SDR) is an emerging research topic where the reconfiguration of transceiver architectures is reached by means of software based projects methodologies[3].for every electronic product lower circuit complexity is always an imported design target since it reduces the cost[4].

In SDR mostly functions are performed by software module i.e. no need to replace the hardware as in case of ASICs. WIMAX has received a great deal of research over past few years due to extensive application. DUC and DDC plays significant role in realization of modern wireless communication system. Up sampler and down sampler are used to change the sampling rate of digital signal in multirate digital signal processing systems. It is widely known that FPGA is one of the best choices for implemented of DDC and DUC.FPGA are used for real time implementation of signal processing algorithm particularly related to communication because of their high speed and accurate performance. The digital signal processing application by using various sampling rates can improve the flexibility of software defined radio. It reduces the need for expensive anti-aliasing filter and enables processing of different types of signals with different sampling rates[5].

II. WIMAX(IEEE802.16)

Wimax(worldwide interoperability for microwave access) is also called IEEE802.16 which specifies air interface of fixed broadband wireless access(BWA) systems supporting multimedia services. The explosive growth of internet over the last decade has led to increasing demand of high speed internet access. Broadband wireless access (BWA) is increasingly gaining popularity as an alternative last mile technology to DSL lines and cable modems. The WIMAX forum (worldwide interoperability for microwave access) is an industry led nonprofit corporation formed to promote and certify compatibility and interoperability of broadband wireless products. The structure of DUC or DDC depends upon conversion ratio required for WIMAX systems the conversion ratio is typically 8 to 10.for this kind of low conversion factor DDC or DUC is typically constructed using FIR filters only and for higher conversion rates CIC filters are normally used. IEEE 802.16d can be applied in NLOS transmission with frequency between 2-11 GHz and in LOS with frequency between 10-66 GHz.designer of WIMAX system need to meet a number of critical requirements such as processing speed, flexibility and time to market and it is these stringent requirements that ultimately drive the choice of hardware platform[6].

III. THE DIGITAL UP CONVERTOR

DUC and DDC are important components of every modern wireless base station designs. DUC are typically used in transmitters to filter, up sample and modulate the signal from baseband to carrier frequency whereas DDC performs the reverse operation demodulate, down sample and filter so that further processing on received signal can be done at low sampling frequencies.

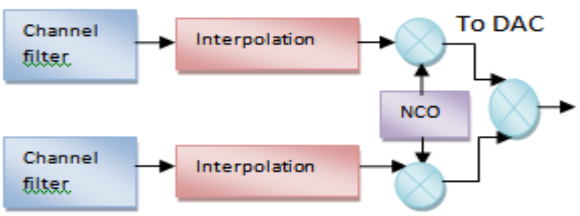

Figure1. Block diagram for DUC

Duc has two basic components pulse shaping which is provided by SR(single rate) FIR filter and interpolation conversion ratio for WIMAX is 8 which is accomplished in two stages of L=2 and L=4 making total 8. For WIMAX input baseband signal has sampling rate of 11.2 MSPS and this signal has to up sample by 8 to achieve IF frequency of 89.6Msps. another method is to design up convertor by using single rate FIR filter and CIC filter which will interpolate the signal factor of 8 by this total number of stages will no doubt will be decreased but the final hardware requirement will be increased . So in order to reduce the hardware we have used three stages first is single rate pulse shaping filter which will ensure that the spectral mask regulations should not be violated. Then second stage is FIR filter having interpolation factor of 2. Then finally FIR filter having interpolation factor of 4 thus making total conversion factor of 8 which is the major requirement.

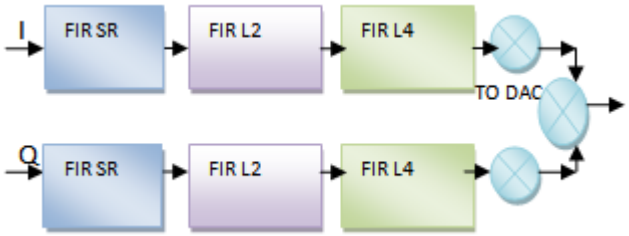

Figure2.Block diagram of DUC with three stages

Different techniques can be used to reduce the number of multipliers on FPGA implementation. We can utilized coefficients symmetry of FIR filters to save multipliers, distributed arithmetic algorithmic operations uses block memory and finally the cascaded integrator comb filters uses the adders instead of multipliers but they are generally used for higher order interpolation factor whereas in case of WIMAX the required interpolation factor is 8 which is too small to use CIC filters. If the interpolation factor is too large suppose N for FIR interpolating filter then it should be broken down to two or three simple cascading filters with N1,N2, N3 interpolation factors but it should satisfy the overall equation: N=N1*N2*N3 it will reduce the total number of taps required to implement the entire filter.

3.1 I**nterpolator**

An up-sampler with up sampling factor L, where L is positive integer develops an output sequence whose sampling rate is L times larger than that of input sequence.

Figure3. Basic Interpolator

Up-sampling operation is implemented by inserting L-1 equidistant zero valued samples between two consecutive samples of X[n].

$$x_u[n] = \begin{cases} x[n/L], & n = 0, \pm L, \pm 2L, \cdots \\ 0, & \text{otherwise} \end{cases} \quad (1)$$

If L=3 then the input signal sampling rate will be increased by twice i.e L-1 as here L is 3 therefore L-1=2 in this case and will insert two zero-valued samples in between the original signal which is further replaced by interpolated values by the interpolater[7].

IV. MATLAB BASED DESIGN AND SIMULATION

The magnitude response of interpolator has been derived from MATLAB. It should satisfy spectral mask regulations otherwise it can cause interference with other spectrums. The filters are designed using MATLAB filter design toolbox. Filter design and analysis tool is a powerful user interface for designing and analyzing filters quickly. FDA tool enables you to design digital FIR or IIR filters by setting filters specifications by importing filters from your MATLAB workspace. FDA tool also provides tools for analyzing filters such as magnitude, phase response, pole zero plots. The transmit spectral mask for WIMAX is defined inIEEE802.16-200standard. Equipment manufacturers of WIMAX are require to ensure that their system comply with spectral mask regulations to prevent interference with other telecommunication devices in order to have interference free communication possible. This lead to requirement that filter and power amplifier must be designed such that no spectral bandwidth beyond allowed channel bandwidth. Both interpolator and decimator can be designed using filter design tool in MATLAB and we have three stages in total for both of these. First we have single rate filter providing the pulse shaping and secondly interpolation by factor of 2 and then interpolation by factor of 4. Single rate filter required very sharp transition so number of taps required will be large as compared to other two stages. The first filter is used to attenuate the spectral energy outside the spectral mask, this filter required the sharpest roll off and hence the maximum numbers of taps. The second filter is associated with rate change of 2 this filter attenuates the spectral images of baseband data in the DUC and applies band limiting in DDC, final stage attenuates the further spectral images and band limiting associated with rate change of stage 4.

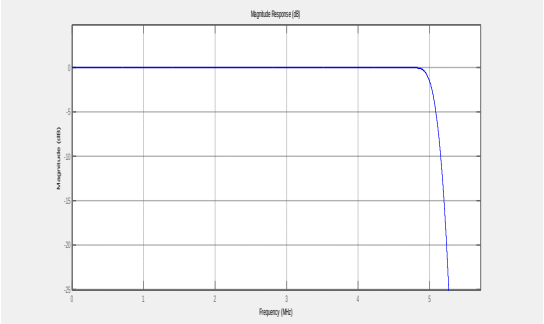

Figure 4. First stage response of single Rate filter.

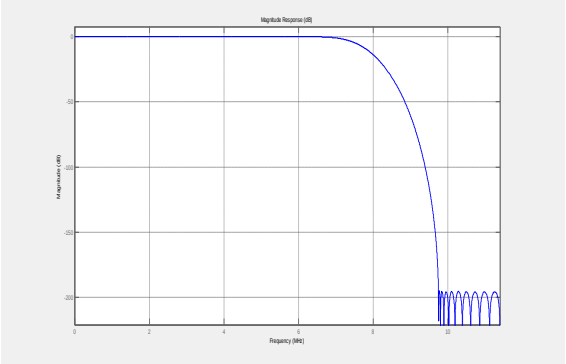

Figure5. Second Stage Response

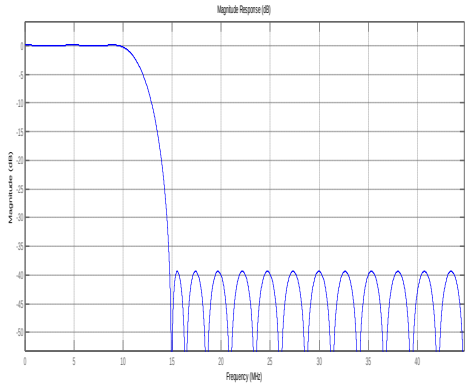

Figure6. Third Stage Response

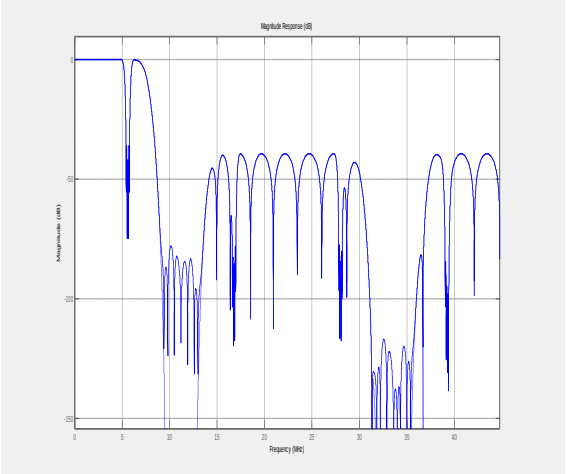

Figure7. Overall Cascaded Response

V. CONCLUSION

In this paper the multistage interpolating filter has been discussed to be used as a part of DUC for WIMAX system. The filters are designed using MATLAB filter design toolbox. Response of all the stages are also shown including single rate, interpolate by 2 and interpolate by 4 and then finally the overall response. Filter design and analysis tool is a powerful user interface for designing and analyzing filters quickly. FDA tool enables you to design digital FIR or IIR filters by setting filters specifications by importing filters from your MATLAB workspace. To meet IEEE 802.16d standard in wireless communication systems we propose cascaded interpolator structure which is based on idea of software defined radio and theorem of multirate signal processing. We can use them for transmitter and receiver in Wimax systems.

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