

## Effect of gate dielectric on threshold voltage of Nanoscale MOSFETS

P.S. Raja<sup>1</sup>, R. Joseph Daniel<sup>2</sup>,

Dept. of E & I Engineering, Annamalai University, Annamalainagar, 608 002,  
Tamilnadu, India.

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**Abstract:** - An integrated circuit (IC) dimensions continue to decrease, RC delay, crosstalk noise, and power dissipation of the interconnect structure become limiting factors for ultra-large-scale integration of integrated circuits. Modern microcircuits may have eight metal layers, each separated by only 0.1 micrometers. RC delays and cross talk rather than transistor speed are now the major performance limitations. The semiconductor industry has responded by developing copper metallization to replace aluminum and lower dielectric constant materials to replace silicon oxide. Materials with different low dielectric constant are being analyzed to replace silicon dioxide as inter level dielectrics. In this paper, how the dielectric constant is affecting the threshold voltage is first discussed. The simulation works are carried using MATLAB, SCHRED software. Based on the results obtained on the effect of k-values on  $V_T$  in nano MOSFETs, the low-k material (PTFE) is suggested as a suitable material for the development of MOSFET as well as interconnects.

**Keywords:** - Threshold voltage, Low-k, Interconnect, MOSFET, PTFE.

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### I. INTRODUCTION

The continuing miniaturization of feature sizes in integrated circuits (ICs) has led to significantly improved device performance and higher packing densities. When feature sizes are reduced beyond 180 nm, however, hundreds of millions of transistors are assembled on a single chip, leading to the increase of RC delay, power consumption, and wire cross-talk between multilevel interconnects [1-4]. As the signal delay from interconnect becomes the limitation of chip performance and reliability [3,5] new materials must be discovered for metal wires and interlayer dielectrics (ILDs). Higher-performance devices could be achieved with the introduction of copper as a low resistivity conductor and new low dielectric constant (k) materials (preferably  $k < 2.0$ ) to replace silicon dioxide ( $k = 3.9$ ). The other side of the story is that the gate oxide required is about 1.2 nm thick and the leakage current at a gate voltage of 1-volt lies between 100 and 1000 A/cm<sup>2</sup> for the 65nm technology node. If the high gate leakage cannot be tolerated, (e.g., portable applications where battery lifetime is a design priority), then the use of high-k gate dielectrics becomes mandatory [6-11]. The high-k dielectrics allow reducing leakage while keeping a very low electrical equivalent oxide thickness (EOT). Recently, the commitment of INTEL and IBM to put hafnium-based high-k gate dielectrics and metal gate electrodes into production for the 45 nm generation leads to major challenges.

Hence, realization of interconnects using low-k dielectric and low leakage gate oxide employing high-k dielectric for the present day electronics with shrinking sizes of semiconductor devices have been reported. However, this implementation is not that easy since the introduction of low k dielectrics poses a greater integration challenge than the introduction of copper metallization and this is reflected by the fact that many device manufacturers have chosen to introduce copper before low k [6,8,15-17]. However, the need for low-k employed interconnects and high k gate oxides and choice of material for these applications have been decided to overcome the physical limits that are to be exercised on the thickness of the Silicon-dioxide. [15-17].

In addition to this, successful scaling of MOSFETs towards shorter channel lengths requires higher doping levels to achieve high drive currents and minimized short-channel effects. All these remedies stand on the basis of semiconductor theory explained by classical mechanics. But as the size goes below 45nm the analysis of MOSFET operation by classical theory and its validity is not known well. For these nanometer devices it was demonstrated a long time ago that, as the oxide thickness is scaled to 10 nm and below, the total gate capacitance is smaller than the oxide capacitance due to the comparable values of the oxide and the inversion layer capacitances. As a consequence, the device transconductance is degraded relative to the expectations of the scaling theory. The inversion layer capacitance was also identified as being the main cause of the second-order thickness dependence of MOSFET's *IV*-characteristics [7]. The finite inversion layer thickness was estimated experimentally by Hartstein and Albert [8]. The high levels of substrate doping, needed in nano-devices to prevent the punch-through effect, that lead to quasi-two-dimensional (Q2D) nature of the

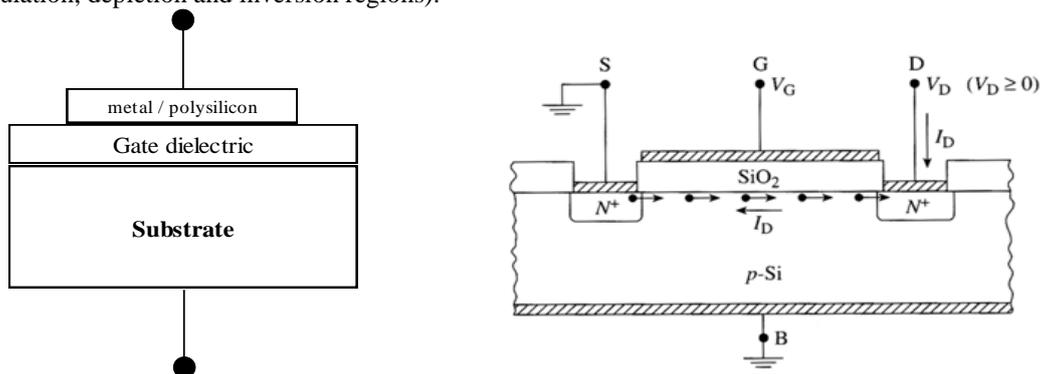
carrier transport, were found responsible for the increased threshold voltage and decreased channel mobility, and a simple analytical model that accounts for this effect was proposed by van Dort and co-workers [9,10]. Later on, Vasileska and Ferry [11] confirmed these findings by investigating the doping dependence of the threshold voltage in MOS capacitors. These results clearly demonstrate the influence of quantum-effects on the operation of nanoscale MOSFETs in both the off- and the on-state. The two physical origins of the inversion layer capacitance, due to the finite density of states and due to the finite inversion layer thickness, were demonstrated experimentally by Takagi and Toriumi [12]. A computationally efficient three-subband model that predicts both the quantum-mechanical effects in the electron inversion layers and the electron distribution within the inversion layer.

The conclusion is that any state-of-the-art simulator should incorporate poly-depletion effects to correctly predict the device off- and on-state behaviour. A simulator must take into consideration the quantum-mechanical nature of the carrier transport and the poly-depletion effects to correctly predict the device off- and on-state behaviour. One such tool that has been successfully utilized in the calculation of the energy level structure in simple MOS or dual-gate capacitor structures is SCHRED that has been developed at Arizona State University and Purdue University and is currently residing on the Purdue NanoHUB. When the situation is like this, it becomes essential to see if the performance of the nanoscale MOSFETs are improved by high-K gate dielectrics and the influence of the low k dielectrics in reducing the inter layer capacitance considering the quantum effects. This can be easily achieved using the simulation software package like SCHRED.

This paper presents the details of a study that focuses in the analysis of threshold voltage of nanoscale MOSFETs employing different gate dielectrics of various k values using classical and quantum theories at different miniaturization scales. The MOSCAP structures and their threshold voltages have been estimated using MATLAB, SCHRED software packages. The results thus obtained are compared to study the role of k-values of dielectrics on threshold voltages and the outcomes of the comparison studies have been presented.

## II. STRUCTURE OF MOSFET/MOS CAPACITOR

The structures of the MOS Capacitors and MOSFETs considered in this study are shown in Figure 1a and 1b respectively. Suppose we build a parallel plate capacitor, where one plate is metal, another plate is a semiconductor (e.g. weakly doped silicon), and the insulator is  $\text{SiO}_2$ . Such a device is called a MOS (metal-oxide-semiconductor) capacitor. The metal plate is called the gate and is not always built out of metal. Nowadays, gates are made from heavily doped polycrystalline silicon (or “Polysilicon” or just “poly”). Polysilicon does not have a rigid crystal lattice and conducts current freely, acting almost like a metal. Since the study of MOS capacitors involve material that is basic in the understanding of MOS transistors, the main building blocks in the fabrication of electronic circuits. That is because the gate of MOS transistor behaves like the MOS capacitor. The usual procedure for characterizing those capacitors and the material properties of the layers forming them is the Capacitance-Voltage (C-V) curve provides the variation of the capacitance with voltage, applied between the metal and silicon layers, for the three main regions of operation of the capacitor (accumulation, depletion and inversion regions).



**Fig. 1.** (a) General construction of MOS – capacitors **Figure.1.** (b) General construction of N-channel MOSFET

A field effect transistor (FET) operates as a conducting semiconductor channel with two ohmic contacts – the *source* and the *drain* – where the number of charge carriers in the channel is controlled by a third contact – the *gate*. The basic MOSFET structure is shown schematically in Figure 1b. In silicon MOSFET, the gate contact is separated from the channel by an insulating silicon dioxide ( $\text{SiO}_2$ ) layer. The charge carriers of the conducting channel constitute an inversion charge, that is, electrons in the case of a  $p$ -type substrate ( $n$ -channel device) or holes in the case of an  $n$ -type substrate ( $p$ -channel device), induced in the semiconductor at the silicon-insulator interface by the voltage applied to the gate electrode. The electrons enter and exit the

channel at  $n+$  source and drain contacts in the case of an  $n$ -channel MOSFET, and at  $p+$  contacts in the case of a  $p$ -channel MOSFET.

### III. METHODOLOGY

In order to study the effect of dielectric on threshold voltage in nanoscale MOSFETs, the analysis was carried out for different dielectric thickness on MOSCAPs using classical mechanics theory, semi classical mechanics and quantum theory. The simulation of MOSCAPs is carried out to obtain the C-V characteristics based on the above said theories. The threshold voltages for various dielectric materials with different substrate doping concentration are extracted from the C-V characteristics obtained for various cases. The various dielectrics considered in this study are PTFE ( $k=2.1$ ), Polyethylene ( $k=2.25$ ) and  $\text{SiO}_2$  ( $k=3.9$ ).

This study focuses on estimating the dependence of threshold voltage on dielectric material, doping concentration of the channel in sub nanoscale devices. Further it becomes important to apply the correct model to estimate the threshold voltage for nano scale devices since the correctness of the device performance evaluated by conventional classical mechanics is a questionable at sub nano meter level. For this reason that the conduction phenomenon at such low scales is not validate. Hence a systematic study using these parameters at nanoscale dimensions becomes important and essentially required. In order to achieve this goal, the following cases have been considered in this study.

**Case (1)** Effect of a selected dielectric material on threshold voltage ( $V_T$ ) for different gate dielectric dimensions for the doping concentration ( $N_A$ ) in the range of  $1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$ .

**Case (2)** Effect of a selected dielectric thickness on  $V_T$  for different dielectric material for the doping concentration in the range of  $1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$ .

**Case (3)** Effect of a selected dielectric thickness and a dielectric material on  $V_T$  for different device theories for the doping concentration in the range of  $1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$ .

For all these cases, the C-V characteristics are obtained at different doping levels of the channel for different combinations as said above. As stated earlier, the doping needs to be kept very high to achieve high drive currents and minimized short-channel effects in nano MOSFETs. Considering this fact, the investigations have been carried out for different doping concentration in the range of  $1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$ . In order to bring out the effect of dielectric on  $V_T$  in nanoscale MOSFETs the above said analysis is carried out for 5nm to 20nm. The different models used in this study include the conventional model for  $V_T$  based on classical mechanics, Berkeley Model that is based on quantum mechanics and SCHRED Classical model and SCHRED quantum model available at <http://www.nanohub.org>. These various models are briefly introduced in the forthcoming section for the convenience of the reader before the results of various analyses are presented.

### IV. THEORITICAL BACKGROUND OF DIFFERENT MODELS OF $V_T$ .

As explained in the methodology the threshold voltages are obtained using different models like the conventional theoretical, BERKELEY, SCHRED Semi classical and SCHRED quantum model.

#### A. Conventional MOSFET theory based on classical mechanics for $V_T$

The threshold voltage of a MOS capacitor is defined as the gate voltage required to cause strong inversion or to make the band bending equal to  $2\phi_f$ . The equation for threshold voltage [12] is written as shown in equation 1.

The threshold Voltage is calculated theoretically as follows:

$$\text{Threshold voltage} \quad V_{th} = \frac{\sqrt{2Q_{ES} \epsilon_0 N_A \phi_s}}{C_{ox}} + 2\phi_f \quad \dots (1)$$

where

$$\text{Threshold voltage} \quad V_{th} = V_{ox} + \phi_s \quad \dots (2)$$

$$\text{Surface potential} \quad \phi_s = 2\phi_f \quad \dots (3)$$

$$\text{Fermi potential} \quad \phi_f = V_t \ln\left(\frac{N_A}{n_i}\right) \quad \dots (4)$$

$$\text{Oxide voltage} \quad V_{ox} = \frac{q \cdot N_A \cdot Wd(\max)}{C_{ox}} \quad \dots (5)$$

$$\text{Depletion width} \quad Wd(\max) = \sqrt{\frac{2\epsilon_s \epsilon_0 \phi_s}{q N_A}} \quad \dots (6)$$

$$\text{Oxide capacitance} \quad C_{ox} = \frac{\epsilon_{ox} \cdot \epsilon_0}{T_{ox}} \quad \dots (7)$$

#### B. BERKELEY Model for $V_T$

This model calculates the capacitance-voltage characteristics of an MOS capacitor considering the electron/hole distributions in both inversion and accumulation modes. These distributions are calculated by solving Schrodinger's and Poisson's equations self-consistently with the Fermi-Dirac distribution using the

physical parameters for (100) Si by a MATLAB software developed by BERKELEY University [18]. The algorithm used in software is described by the flow chart as shown in figure 2.

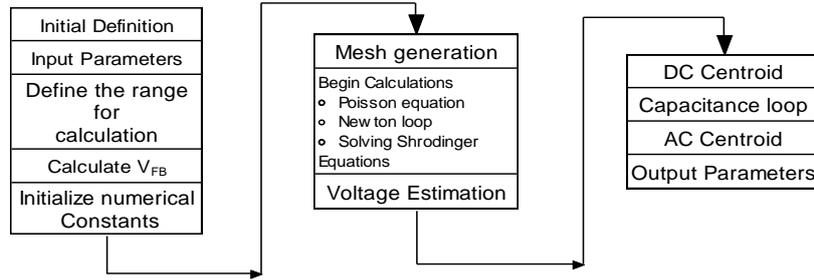


Figure 2. Algorithm for Calculating  $V_{th}$  of a MOS Capacitor Using BERKLEY Model.

### C. The SCHRED model for $V_T$

SCHRED calculates the envelope wave functions and the corresponding bound-state energies in typical metal oxide semiconductor (MOS), silicon-on-substrate(SOS) or silicon-on-insulator (SOI) structures by solving self-consistently the one-dimensional (1D) Poisson equation and the 1D Schrödinger equations. The important features of SCHRED model is that it can simulate both p type and n type silicon bodies for bulk or SOI structures and can assume both n-type and p-type polysilicon or metals with specified work function as the gate contact. It gives the flexibility to estimate  $V_T$  in both classical and quantum modes. Further the user can select either Maxwell-Boltzmann or Fermi-Dirac statistics in the classical simulation mode and SCHRED assumes the [100] plane to be parallel to the Si/SiO<sub>2</sub> interface in quantum simulation mode.

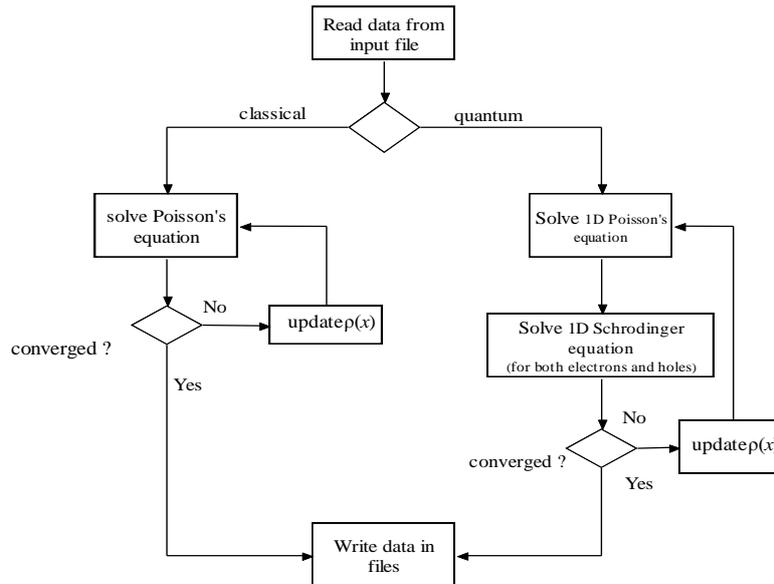


Figure 3. Algorithm used in SCHRED model

It gives a wide range of outputs like conduction-band edge profile, charge density per cm<sup>3</sup> and per cm<sup>2</sup> in the body, average distance of carriers from the interface, total gate capacitance  $C_{tot}$ , and oxide capacitance  $C_{ox}$ . It also provides the subband energies and wave functions in the body when the quantum mode simulation is chosen. Figure. 3 shows the algorithm used in SCHRED model in both simulation modes.

## V. C-V CHARACTERISTICS OF MOSFETS

The C-V characteristics of MOSCAPs using various dielectrics at the different doping levels are obtained by all the four different theories as described in the previous sections. The threshold voltages extracted from these CV characteristics are presented and discussed here for the doping range of  $N_A = 1 \times 10^{15} / \text{cm}^3$  to  $1 \times 10^{21} / \text{cm}^3$ .

### A. Effect of a selected dielectric material on $V_T$ for different gate dielectric dimensions

In this section the focus is the effect of a dielectric material on  $V_T$  at various thickness of the dielectrics. The threshold voltages have been obtained using all the four models.

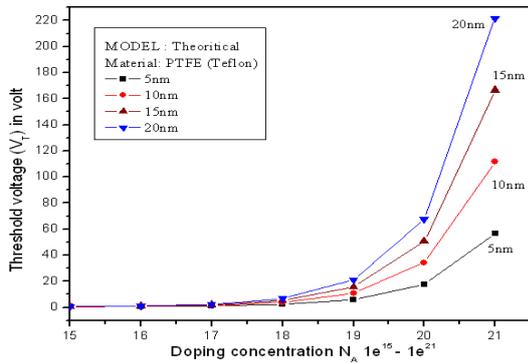
### 1) Conventional inversion mode Model

The effect of low-k dielectric on the threshold voltage has been studied by simulation of MOSCAPs with a doping concentration in the range of  $N_A=1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$  and compared with the MOSCAPs with  $\text{SiO}_2$  as dielectric thickness. The authors have considered the different dielectric thickness viz. 5nm, 10nm, 15nm and 20nm. The threshold voltage values have been obtained using MATLAB with different thickness for PTFE, Polyethylene and  $\text{SiO}_2$  has shown in Table 1.

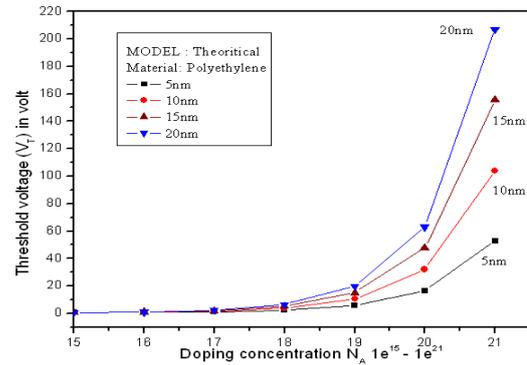
**Table 1:** Calculated  $V_{Th}$  of a MOS Capacitor using conventional theoretical method.

order of doping $N_A$	PTFE (k=2.1) $V_{Th}$ (in Volt) for various Dielectric thickness				Polyethylene (k =2.25) $V_{Th}$ (in Volt) for various Dielectric thickness				$\text{SiO}_2$ (k=3.9) $V_{Th}$ (in Volt) for various Dielectric thickness			
	5nm	10nm	15nm	20nm	5nm	10nm	15nm	20nm	5nm	10nm	15nm	20nm
15	0.6	0.6	0.7	0.7	0.6	0.6	0.7	0.7	0.56	0.59	0.61	0.63
16	0.8	0.9	1.1	1.2	0.8	0.9	1	1.1	0.74	0.81	0.87	0.95
17	1.2	1.7	2.1	2.5	1.2	1.6	2	2.4	1.02	1.26	1.49	1.73
18	2.4	3.9	5.3	6.8	2.3	3.7	5.1	6.4	1.67	2.5	3.29	4.09
19	6	11	15.9	20.9	5.7	10.3	15	19.6	3.7	6.38	9.05	11.74
20	17.7	34.3	50.9	67.6	16.6	32.1	47.6	63.1	10.07	19.01	27.95	36.88
21	56.4	111.5	166.6	221.7	52.7	104.1	155.6	207	30.9	60.6	90.3	120.0

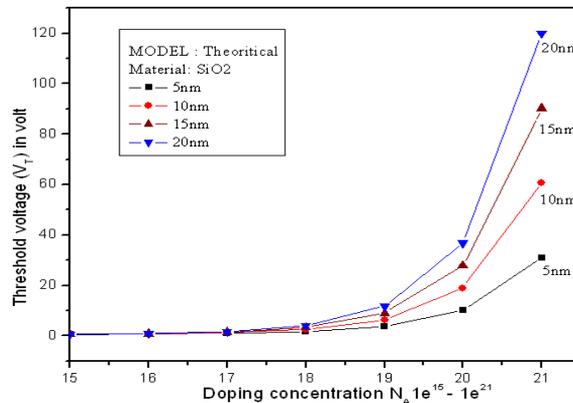
By employing conventional theoretical model as said in section 3 the threshold voltage of a MOSCAP using the dielectric materials viz PTFE, Polyethylene, and  $\text{SiO}_2$  at different oxide thickness was obtained and plotted. The  $V_T$  comparison plotted for PTFE, polyethylene and  $\text{SiO}_2$  are shown in the figure 4a, 4b and 4c respectively. It is observed that the threshold voltages remain almost constant irrespective of dielectric constant and thickness for the doping region of  $1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{18}/\text{cm}^3$ , with a deviation of a 65% maximum. It is also seen that these values for very high doping are impractical.



**Figure.4.(a)** Comparison of  $V_T$  obtained at  $T_{ox}=5\text{nm}, 10\text{nm}, 15\text{nm}, 20\text{nm}$  for PTFE with substrate doping  $N_A=1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$  using conventional model



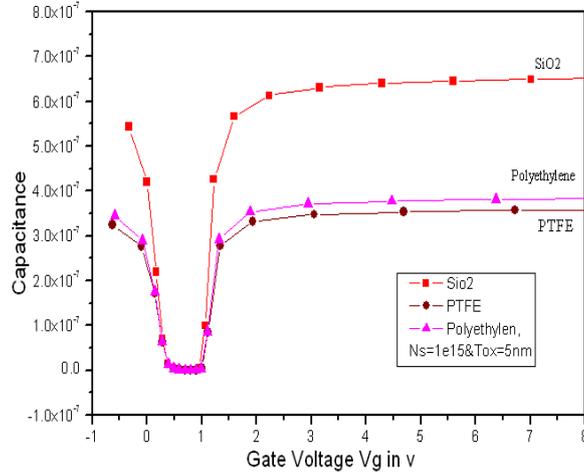
**Figure.4.(b)** Comparison of  $V_T$  obtained at  $T_{ox}=5\text{nm}, 10\text{nm}, 15\text{nm}, 20\text{nm}$  for polyethylene with substrate doping  $N_A=1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$  using conventional model



**Figure.4.(c)** Comparison of  $V_T$  obtained at  $T_{ox}=5\text{nm}, 10\text{nm}, 15\text{nm}, 20\text{nm}$  for  $\text{SiO}_2$  With substrate doping  $N_A=1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$  using conventional model.

2) **BERKELEY Model**

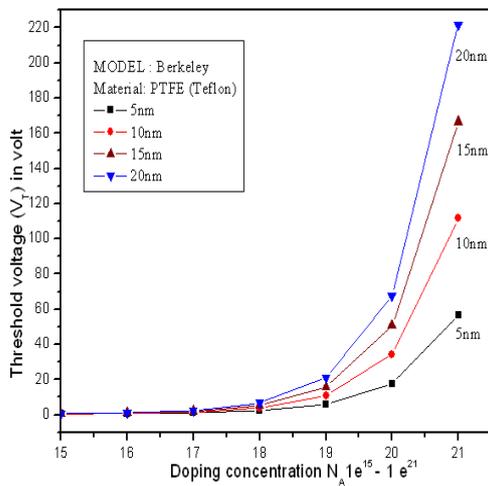
In BERKELEY model the MATLAB program was executed to obtain the C-V graph of the MOSCAP using the various dielectric materials PTFE, Polyethylene, and SiO<sub>2</sub> at dielectric thickness of 5,10,15 and 20nm. The C-V characteristics of MOSCAP having a doping concentration value of  $1 \times 10^{15}/\text{cm}^3$  and with the dielectric thickness of 5nm employing SiO<sub>2</sub>, Polyethylene and Teflon is shown in Figure 5. From the obtained C-V characteristics the threshold voltage ( $V_T$ ) was extracted and were tabulated separately.



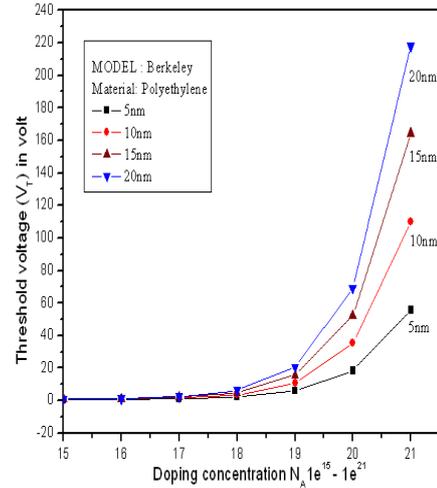
**Figure: 5** C-V curve of PTFE, Polyethylene, SiO<sub>2</sub>

For Tox=5nm with substrate doping as  $N_A=1 \times 10^{15}/\text{cm}^3$  using BERKELEY model

The various threshold voltages  $V_T$  comparison plotted for PTFE and Polyethylene and SiO<sub>2</sub> are as shown in the figure 6a, 6b and 6c respectively. These results also follow the same trend as seen in the results obtained using classical mechanics. The threshold voltages are almost same for  $1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{18}/\text{cm}^3$ , with a deviation of a 56% maximum.

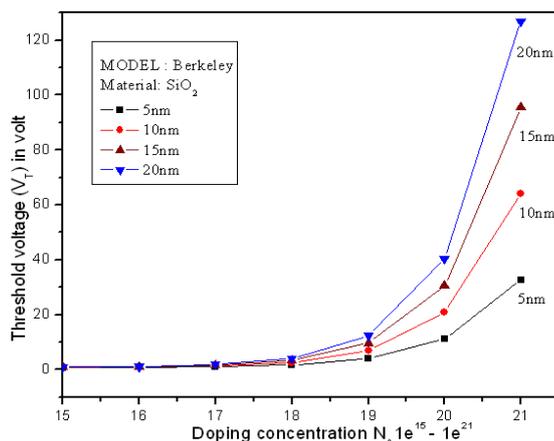


**Figure.6.(a)** Comparison of  $V_T$  obtained at Tox=5nm, 10nm, 15nm, 20nm for PTFE with substrate doping  $N_A$



**Figure.6.(b)** Comparison of  $V_T$  obtained at Tox=5nm, 10nm, 15nm, 20nm for polyethylene with substrate doping  $N_A$

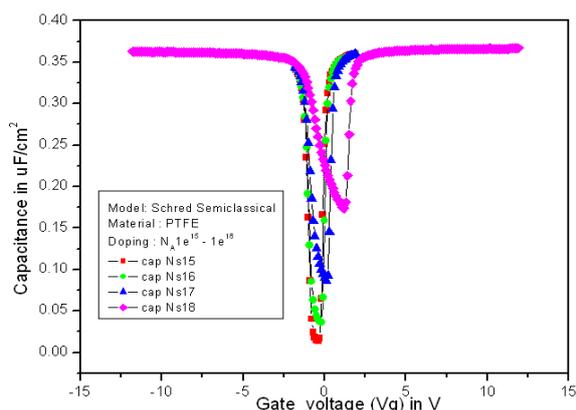
$=1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$  using BERKELEY model  $N_A=1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$  using BERKELEY model



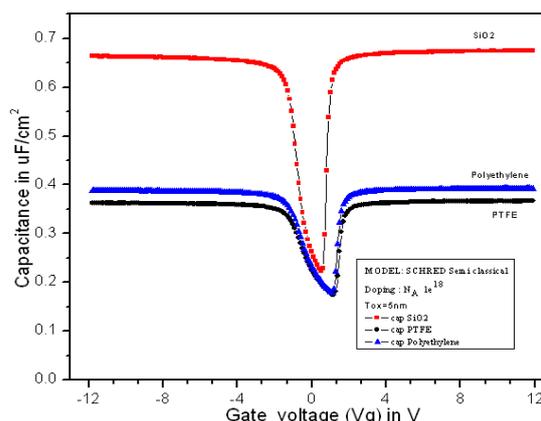
**Figure.6.(c)** Comparison of  $V_T$  obtained at  $T_{ox}=5\text{nm}, 10\text{nm}, 15\text{nm}, 20\text{nm}$  for  $\text{SiO}_2$  With substrate doping as  $N_A=1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$  using BERKELEY model.

### 3) SCHRED Semi Classical Model

In Semi Classical model the SCHRED software [19] was executed and obtained the C-V graph of the MOSCAP with the various dielectric materials PTFE, Polyethylene and  $\text{SiO}_2$  at different oxide thickness value of 5,10,15 and 20nm. From the C-V graph the threshold voltages for the various dielectric materials at different oxide thickness were extracted and tabulated.

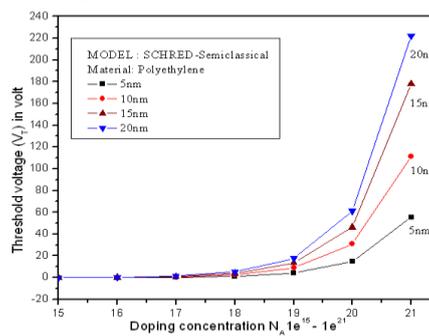
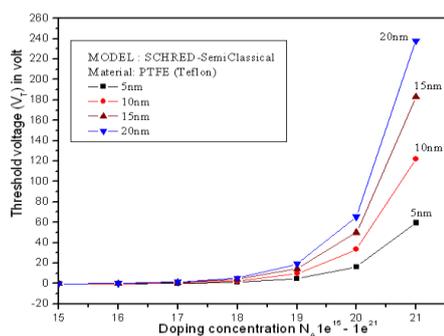


**Figure: 7a** C-V curve of PTFE for  $T_{ox}=5\text{nm}$  With substrate doping as  $N_A=1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{19}/\text{cm}^3$  using SCHRED Semi classical model

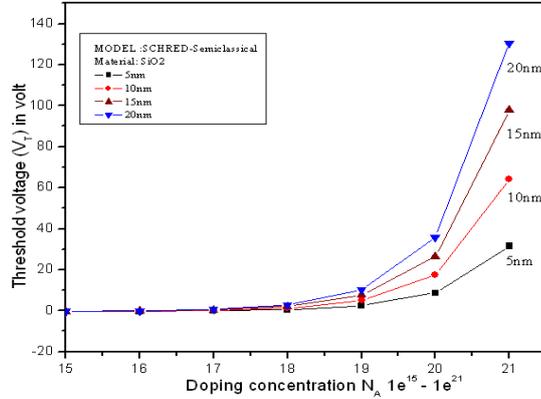


**Figure: 7b** C-V curve of PTFE, Polyethylene,  $\text{SiO}_2$  with  $T_{ox}=5\text{nm}$  and substrate doping as  $N_A$  to  $1 \times 10^{21}/\text{cm}^3$  using SCHRED Semi classical model

The  $V_T$  comparison plotted for PTFE and Polyethylene and  $\text{SiO}_2$  under the semi classical theory is as shown in the figure 8a, 8b and 8c. It is observed that the threshold voltages remain almost constant irrespective of dielectric constant and thickness for the doping region of  $1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{19}/\text{cm}^3$ , with a deviation of a 60% maximum. It is also seen that these values for very high doping are impractical.



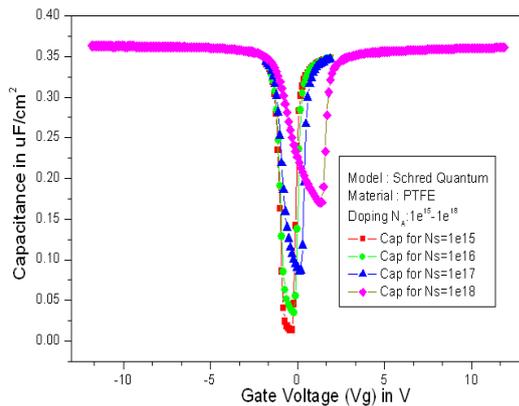
**Figure.8.(a)** Comparison of  $V_T$  obtained at  $T_{ox}=5\text{nm}$ , **Figure.8.(b)** Comparison of  $V_T$  obtained at  $T_{ox}=5\text{nm}$ , 10nm, 15nm, 20nm for PTFE with substrate doping  $N_A$  10nm, 15nm, 20nm for polyethylene with substrate doping  $N_A=1\times 10^{15}/\text{cm}^3$  to  $1\times 10^{21}/\text{cm}^3$  using SCHRED classical semi classical model.



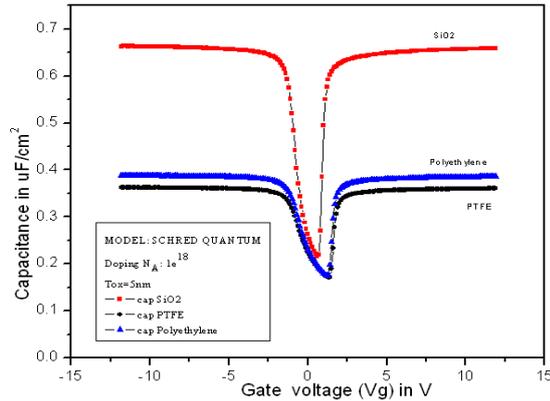
**Figure.8.(c)** Comparison of  $V_T$  obtained at  $T_{ox}=5\text{nm}, 10\text{nm}, 15\text{nm}, 20\text{nm}$  for  $\text{SiO}_2$  with substrate Doping as  $N_A=1\times 10^{15}/\text{cm}^3$  to  $1\times 10^{21}/\text{cm}^3$  using SCHRED Semiclassical model.

#### 4) SCHRED Quantum Model

Similar to the semi classical method the C-V graph was obtained for quantum model also.



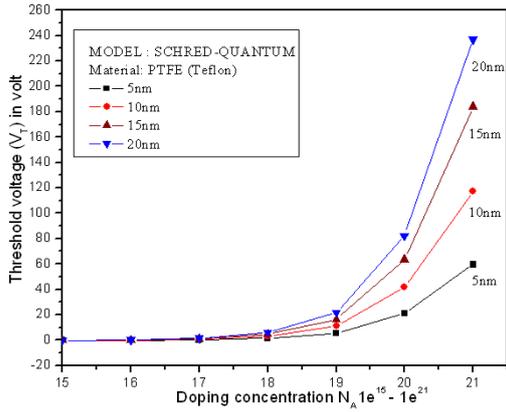
**Figure:9a** C-V curve of PTFE for  $T_{ox}=5\text{nm}$  with substrate doping as  $N_A=1\times 10^{15}/\text{cm}^3$  to  $1\times 10^{21}/\text{cm}^3$  using SCHRED quantum model



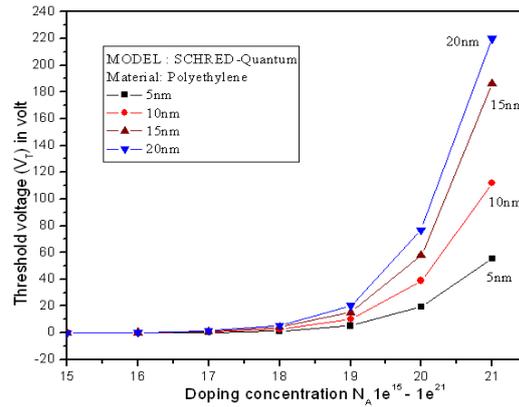
**Figure: 9b** C-V curve of PTFE, Polyethylene,  $\text{SiO}_2$  with  $T_{ox}=5\text{nm}$  and substrate doping as  $N_A$  to  $1\times 10^{21}/\text{cm}^3$  using SCHRED quantum model.

The C-V characteristics of MOSCAP using the dielectric material as PTFE thickness of 5nm in the range of doping concentration  $1\times 10^{15}/\text{cm}^3$  to  $1\times 10^{18}/\text{cm}^3$  has been shown in Figure 9a. The C-V characteristics of MOSCAP using the dielectric material PTFE, Polyethylene and  $\text{SiO}_2$  with dielectric thickness of 5nm in the doping concentration of  $1\times 10^{18}/\text{cm}^3$  has been shown in Figure 9b.

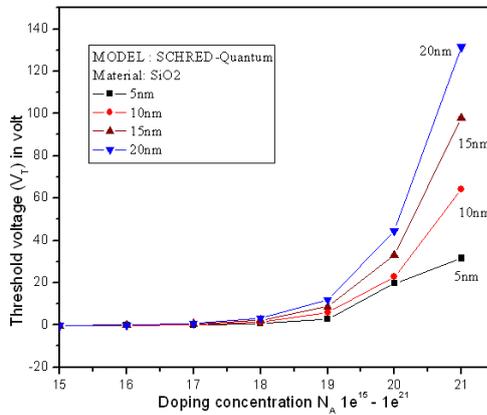
From the various C-V graphs the threshold voltage for the different dielectric materials PTFE, Polyethylene, and  $\text{SiO}_2$  at different oxide thickness was extracted and tabulated. The  $V_T$  comparison plotted for PTFE and Polyethylene and  $\text{SiO}_2$  under the SCHRED quantum model are shown in the figure 10a, 10b and 10c. It is observed that the threshold voltages remain almost constant irrespective of dielectric constant and thickness for the doping region of  $1\times 10^{15}/\text{cm}^3$  to  $1\times 10^{19}/\text{cm}^3$ .



**Fig.10a.** Comparison of  $V_T$  obtained at  $T_{ox}=5\text{nm}$ ,  $10\text{nm}$ ,  $15\text{nm}$ ,  $15\text{nm}$ ,  $20\text{nm}$  for PTFE with substrate doping  $N_A=1\times 10^{15}/\text{cm}^3$  to  $1\times 10^{21}/\text{cm}^3$  using SCHRED quantum mode



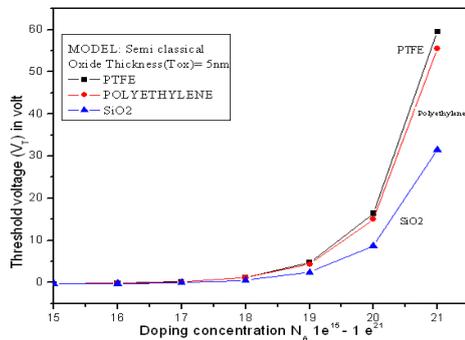
**Fig.10b.** Comparison of  $V_T$  obtained at  $T_{ox}=5\text{nm}$ ,  $10\text{nm}$ ,  $15\text{nm}$ ,  $15\text{nm}$ ,  $20\text{nm}$  for Polyethylene with substrate doping  $N_A=1\times 10^{15}/\text{cm}^3$  to  $1\times 10^{21}/\text{cm}^3$  using SCHRED quantum



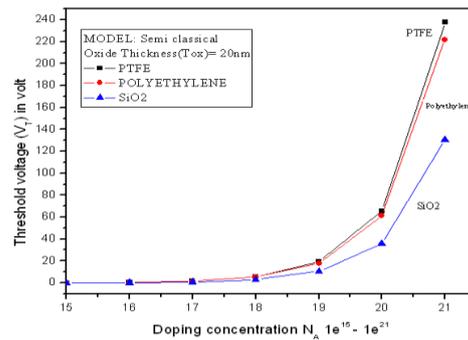
**Figure.10.(c)** Comparison of  $V_T$  obtained at  $T_{ox}=5\text{nm}$ ,  $10\text{nm}$ ,  $15\text{nm}$ ,  $20\text{nm}$  for  $\text{SiO}_2$  with Substrate doping as  $N_A=1\times 10^{15}/\text{cm}^3$  to  $1\times 10^{21}/\text{cm}^3$  using SCHRED quantum model.

**B. Effect of a selected oxide thickness on  $V_T$  for different dielectric material**

In the second case (case ii) we have considered the comparison of different dielectric materials at selected oxide thickness. The comparison of different dielectric materials under SCHRED semi classical model with an oxide thickness of  $5\text{nm}$  and  $20\text{nm}$  are shown in the figure 11a and 11b.



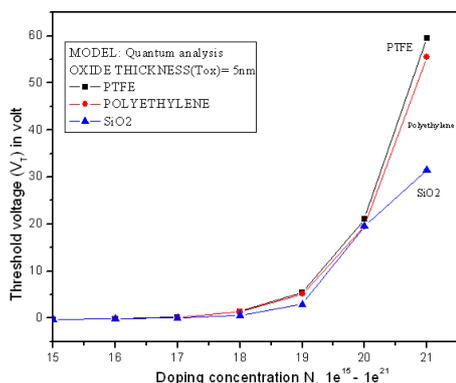
**Figure : 11a** Comparison of  $V_T$  for different dielectric materials at  $T_{ox} = 5\text{nm}$  with substrate doping as  $N_A=1\times 10^{15}/\text{cm}^3$  to  $1\times 10^{21}/\text{cm}^3$  using SCHRED semi classical model.



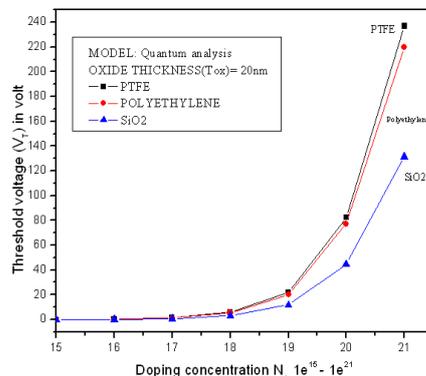
**Figure : 11b** Comparison of  $V_T$  for different materials at  $T_{ox} = 20\text{nm}$  with substrate doping as  $1\times 10^{15}/\text{cm}^3$  to  $1\times 10^{21}/\text{cm}^3$  using SCHRED semi classical

Model.

Similarly the comparison of different dielectric materials under SCHRED quantum model with an oxide thickness of 5nm and 20nm are shown in the figure 12a and 12b.



**Figure : 12a** Comparison of  $V_T$  for different dielectric materials at  $T_{ox} = 5\text{nm}$  with substrate doping as  $N_A = 1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$  using SCHRED quantum model.



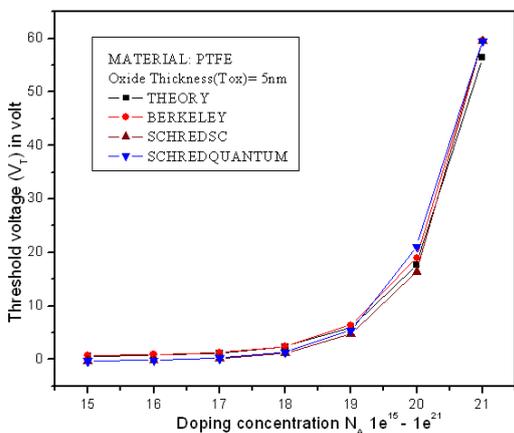
**Figure : 12b** Comparison of  $V_T$  for different materials at  $T_{ox} = 20\text{nm}$  with substrate doping as  $N_A = 1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$  using SCHRED quantum model.

Model.

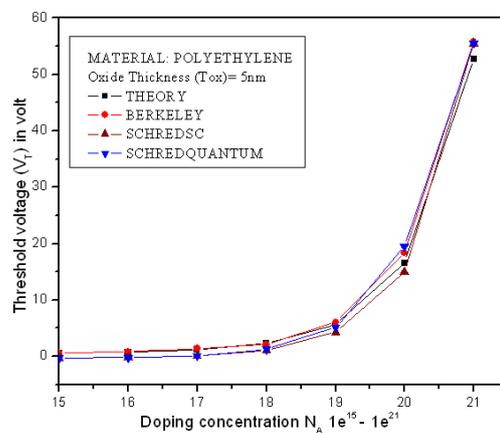
From the above graph we can observe that the threshold voltage ( $V_T$ ) for the different dielectric materials are also be constant in the doping concentration range of  $1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{19}/\text{cm}^3$  for the oxide thickness range of 5nm to 20 nm.

**C. Effect of a selected oxide thickness and a dielectric material on  $V_T$  for different device theories**

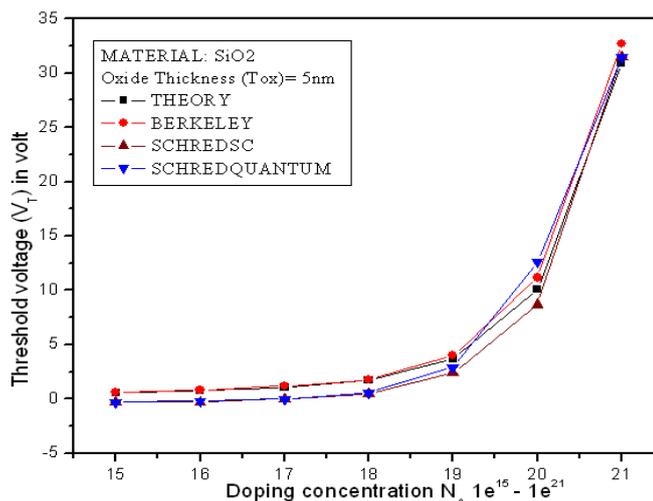
In the third case (case iii) we have considered the comparison of different device theories for selected dielectric material with selected oxide thickness. The comparison of conventional model, BERKELEY model, SCHRED semi classical model, SCHRED quantum model for PTFE, Polyethylene and  $\text{SiO}_2$  at 5nm oxide thickness are shown in the figure 13a, 13band 13c respectively.



**Figure: 13a** Comparison of different device model For PTFE at  $T_{ox} = 5\text{nm}$  with substrate doping as  $N_A$  as  $N_A = 1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$



**Figure: 13b** Comparison of different device model for Polyethylene at  $T_{ox} = 5\text{nm}$  with substrate doping  $N_A = 1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$ .



**Figure.13.** (c) Comparison of different device model for  $\text{SiO}_2$  at  $T_{\text{ox}}=5\text{nm}$  with Substrate doping as  $N_A=1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{21}/\text{cm}^3$ .

From the above graph we can observe that the threshold voltage ( $V_T$ ) for the different device models for a particular dielectric material is also be constant in the doping concentration range of  $1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{19}/\text{cm}^3$  for a particular dielectric thickness.

## VI. CONCLUSION

The effect of low-k dielectrics on the MOSFET characteristics have been studied extensively. The results obtained using various models show that the threshold voltages at different doping concentration remains almost the same irrespective of the “k” of various dielectric materials with ( $K < 4$  ( $\text{SiO}_2$ )). This phenomenon is seen only upto  $1 \times 10^{19}/\text{cm}^3$ . Beyond this  $> 10^{19}/\text{cm}^3$ , the threshold voltages increased with doping concentration irrespective of the “k” value of the dielectric material. Similarly in this doping region of  $1 \times 10^{15}/\text{cm}^3$  to  $1 \times 10^{19}/\text{cm}^3$  the threshold voltage remains almost the same for various dielectric thicknesses in the range of 5nm to 20nm irrespective of the material. It is also seen that the threshold voltages obtained by various models seem to be matching closely.

## REFERENCES

- [1]. Mehdi Moussavi “Advanced Interconnect schemes towards 0.1 $\mu\text{m}$ ” 1999 IEEE.
- [2]. D. Neyl, V. Girault, X. Federspiel, “Analytical extraction of thermal conductivities of low-k dielectrics for advanced technologies 2004 IRW final report.
- [3]. R. Singh, R.Sharangpani, K. F. Poole, and M.M. Moslehi, “Critical Technology Challenges in Low Power Electronics” 1995 IEEUSEMI Advanced Semiconductor Manufacturing Conference.
- [4]. M. Tagami<sup>1</sup>, H. Ohtake<sup>1</sup>, M. Tada<sup>1</sup>, M. Ueki<sup>1</sup>, F. Ito<sup>1</sup>, T. Taiji, Y. Kasama, T. Iwamoto, H. Wakabayashi<sup>1</sup>, T. Fukai, “High-performance Cu-interconnects with Novel Seamless Low-k SiOCH Stacks (SEALS) Featured by Compositional Modulation Process for 45nm-node ULSI Devices” 2006 Symposium on VLSI Technology Digest of Technical Papers (c) 2006 IEEE.
- [5]. C. Guedjrx, L. baud, M. Fayolle, V. Jousseau, J.F. Guillaumond, J. Cluzel, A. Toffoli t, G.Reirnbold, D. Bowhu “Effect of pore sealing on the reliability of ULWCu interconnects” 2004 IEEE.
- [6]. E.Josse, S.Parihar, O.Callen, P.Ferreira, C.Monget, A.Farcy, “A Cost-Effective Low Power Platform for the 45-nm Technology Node” STMicroelectronics.
- [7]. Nobuo Aoi, Eiji Tamaoka, Michinari Yamanaka, Shuji Hirao, Tetsuya Ueda, and Masafumi Kubota, “A Novel Clustered Hard Mask Technology for Dual Damascene Multilevel Interconnects with Self-Aligned Via Formation Using an Organic Low k Dielectric” ULSI Process Technology Development Center, Semiconductor Group, Matsushita Electronics Corporation.
- [8]. Ashwani Kumar, Narottam Chand ,Vinod Kapoor, “A Compact Gate Tunnel Current Model for Nano Scale MOSFET with Sub1nm Gate Oxide” International journal of applied engineering research, dindigul Volume 1, No1, 2010
- [9]. Chung-Hui Chen a, Yean-Kuen Fang a, Chun-Sheng Lin a, Chih-Wei Yang a, Jang-Cheng Hsieh , “A novel multi-level interconnect scheme with air as low K inter-metal dielectric for ultradeep submicron application” Solid-State Electronics, 2001.

- [10]. C.F. Tsang, Y.J. Su, V.N. Bliznetsov and G.T. Ang, "130nm Process Technology Integration of Advanced Cu/CVD Low k Dielectric Material - Case Study of Failure Analysis and Yield-Enhancement" IEEE. Proceedings 2003, Singapore.
- [11]. S. Parihar, M. Angyal, B. Boeck, "A High density 0.10um CMOS technology using low-k dielectric and copper interconnect" ,2001, IEEE.
- [12]. M.K. Achuthan and K.N.Bhat, "Fundamentals of Semiconductor Devices", Tata McGraw-Hill Publications, New Delhi, 2007.
- [13]. Dan Blanks, Gerhard Klimeck, Roger Lake, R. Chris Bowen, William R. Frensley, Manhua Leng, and Chenjing L. Fernando, "Nanoelectronic Modeling (NEMO): A New Quantum Device Simulator".
- [14]. *Navakanta Bhat*, "Nanoelectronics Era: Novel Device Technologies Enabling SystemsonChips" Journal of the Indian Institute of Science, Jan-Mar 2007
- [15]. Chioko Kaneta, Takahiro Yamasaki, Yuko Kosaka "Nanoscale simulation for advanced gate dielectrics" Manuscript January14, 2003.
- [16]. P.K.Vasudev, "CMOS device and interconnect technology enhancements for low power/low voltage applications" solid-state electronics vol. 39, 1996.
- [17]. R.J.O.M. Hoofman, G.J.A.M. Verheijden, J. Michelon, F. Iacopi, Y. Travaly, M.R. Baklanov, Zs. Tokei, G.P. Beyer, "Challenges in the implementation of low-k dielectrics in the back-end of line" Microelectronic Engineering,2005.
- [18]. <http://www-device.eecs.berkeley.edu>.
- [19]. [www.nanohub.org](http://www.nanohub.org)