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A Novel Method for the Elimination of Dead Time in Two Level Voltage Source Inverter

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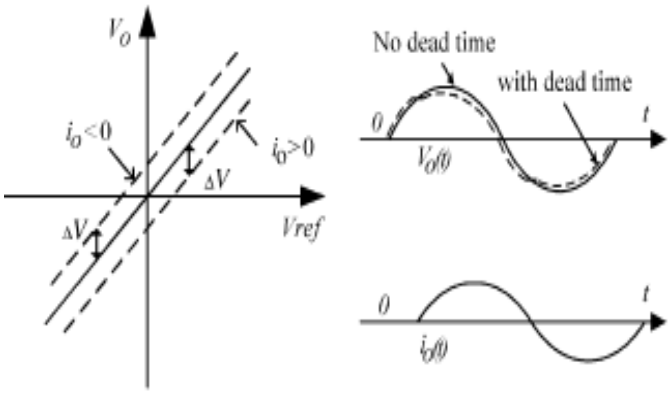
Abstract: - Dead time is a short delay introduced between the gating signals of the upper and lower switches in an inverter leg to prevent the short circuit of dc link. Such dead time results in a change in f undamental voltage and also causes low frequency distortion. In this paper , a novel method for the elimination of dead time in two level voltage source inverter is proposed and implemented. This method reduces the low frequency distortion and results in a steady fundamental voltage. The validity of this method has been studied by the PSPICE Simulation and prototype experiment.

Keywords: - Dead-time, harmonic, phase-leg, gate drive, voltage source inverter (VSI)

I. INTRODUCTION

To avoid shoot-though in PWM controlled voltage source inverters (VSI), dead-time, a small interval during which both the upper and lower switches in a phase leg are off, is introduced into the control of the standard VSI phase leg. However, such a blanking time can cause problems such as output waveform distortion and fundamental voltage loss inVSIs.[1-4].Fig. 1(a) shows the dead-time effect in a voltage source inverter.



(a) **(b)**

Fig.1. Effect of dead time

Fig 1 (b) shows the output voltage waveform distortion caused by dead-time effect. To overcome dead-time effects, most solutions focus on dead-time compensation [1-4] by introducing complicated PWM controller and expensive current detection hardware. In practice, the dead-time varies with the devices and output current, as well as temperature, which makes the compensation less effective, especially at low output current, low frequency, and zero current crossing. [5] proposed a new switching strategy for PWM power converters. [6] presented an IGBT gate driver circuit to eliminate the dead-time effect. [7] proposed a phase leg configuration topology which prevented shoot through. However, an additional diode in series in the phase leg increases complexity and causes more loss in the inverter. Also, this phase leg configuration is not suitable for high power inverters because the upper device gate turn off voltage is reversely clamped by a diode turn on voltage. Such a low voltage, usually less than 2 V, is not enough to ensure that a device is in off state during the activation of its complement device.[7]

II. PRINCIPLE OF DEAD TIME ELIMINATION

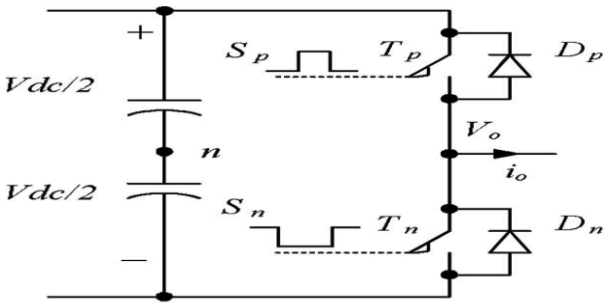


Fig. 2. A generic phase leg of VSIs.

To explain the principle of the proposed dead-time elimination method, we refer to a generic phase leg of VSIs, as shown in figure 2. Assuming the output current flows out of the phase leg, in each switching cycle, the current comes out from the upper device when *Kp* is on and freewheels through diode *Dn* when *Kp* is off. Here this current direction is defined as positive. Under this condition, the generic phase leg can be equivalently expressed as a P type switching cell. Similarly when load current flows into the phase leg, defined as negative, the current goes into the lower device when *Kn* is on and freewheels through diode *Dp* when *Kn* is off. Under this condition, the generic phase leg can be equivalently expressed as a N type switching cell . Actually a generic phase leg is a combination of one P switch cell and one N switch cell. There is no question that dead-time is not required for either a P switch cell or a N switch cell because both cells are configured with a controllable switch in series with a uncontrollable diode.[8].

III. TWO LEVEL VOLTAGE SOURCE INVERTER

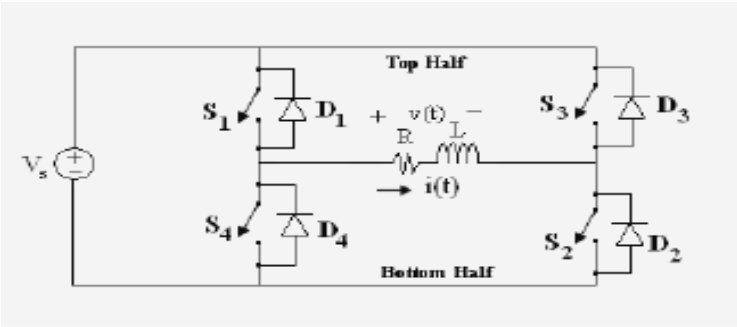


Fig.3.Full-bridge inverter feeding an RL load

The full-bridge circuit feeding an inductive (RL) load is shown in fig.3. A simple scheme of controlling the gating of the four switches is also shown. Although each switch is gated to be on for one-half the time period, each switch may not conduct for one-half the time period due to the constraints imposed by the load. The arrow-head shows the direction in which the current can flow through each switch. When a switch is gated on but the current is in the opposite direction, the freewheeling diode placed in anti parallel with the switch will provide the path for the current. Note that there are two intervals during which the output voltage is zero. During the time interval between a and b, the current i(t) circulates in the top-half of the circuit through S_1 and D_3 and the voltage across the load is zero assuming the diode and the switch are ideal. Likewise, the current completes it path through S_4 and D_2 in the bottom half of the circuit during the time interval from c to d and the voltage across the load is zero.

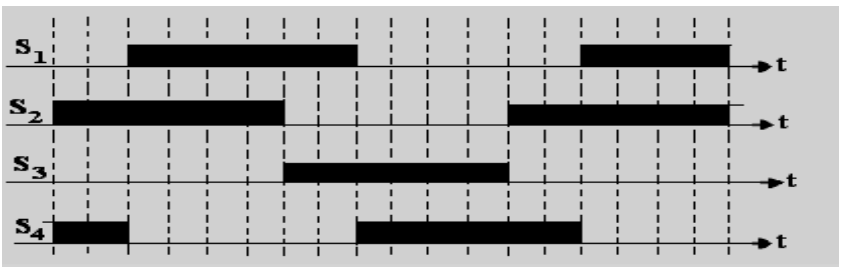


Fig. 4. Waveform for the gating scheme of the 4 switches

IV. SIMULATION RESULTS

In this paper, the simulation model is developed with PSPICE tool which contains a dc source, four MOSFETs , inductor, capacitor and a resistive load. The MOSFET is driven by the gate signal of frequency of 50KHZ. The circuit is designed for an output of 40V with an input of 48V. The simulation circuit of the proposed method and the output voltage waveform is shown in fig.5. and fig.6.

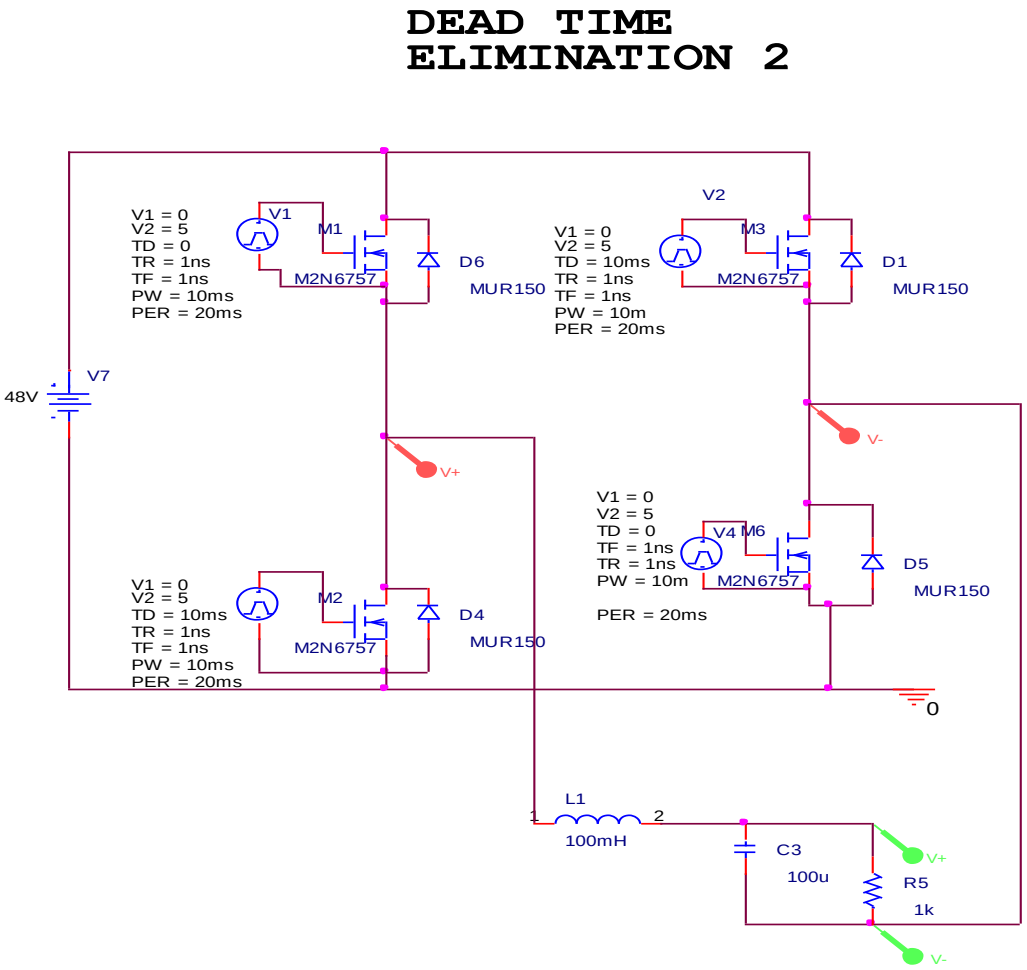


Fig.5. Simulation circuit of the proposed method

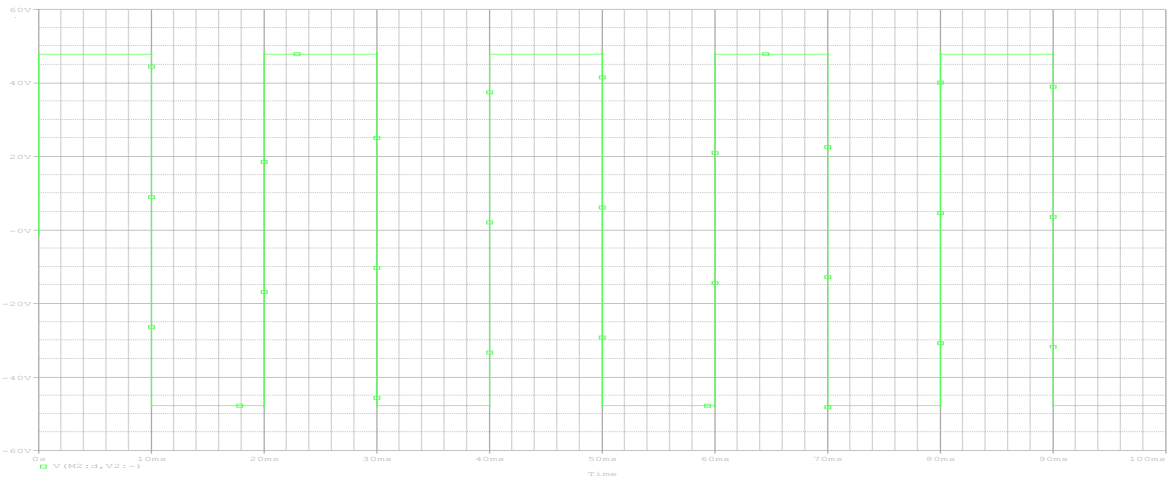


Fig.6. Output Voltage Waveform

In this proposed method, the dead time effect has been dramatically minimized and the output distortion also reduces.

V. HARDWARE IMPLEMENTATION

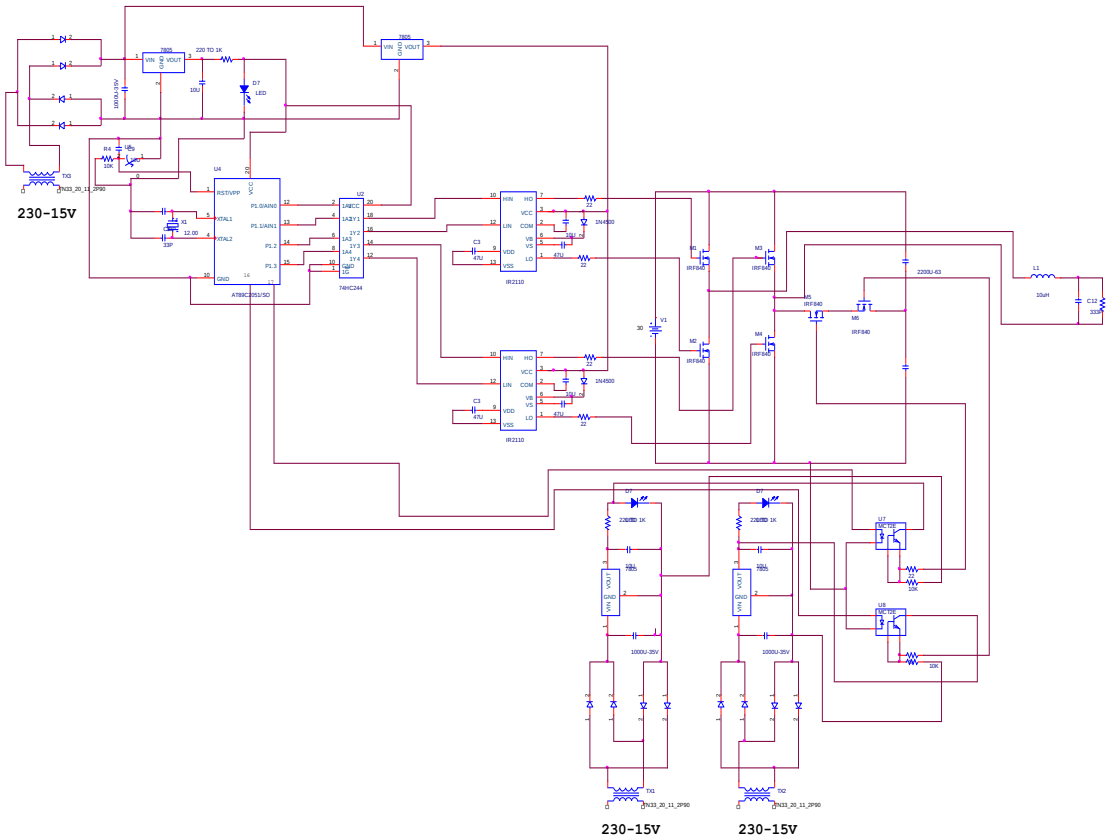


Fig.7. Hardware circuit diagram

The hardware circuit for the proposed method is shown in fig.7. The hardware circuit consists of the following major parts such as power supply unit, microcontroller circuit, buffer circuit and isolation circuit. Fig.8. shows the power and control circuit.

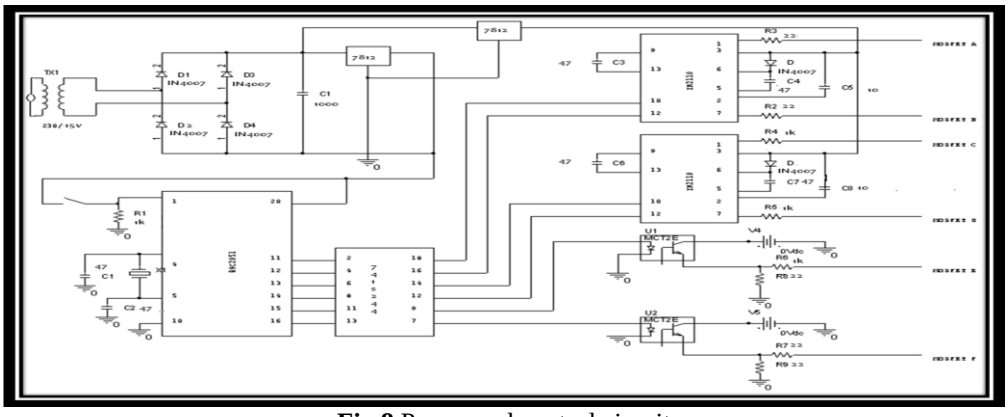


Fig.8. Power and control circuit

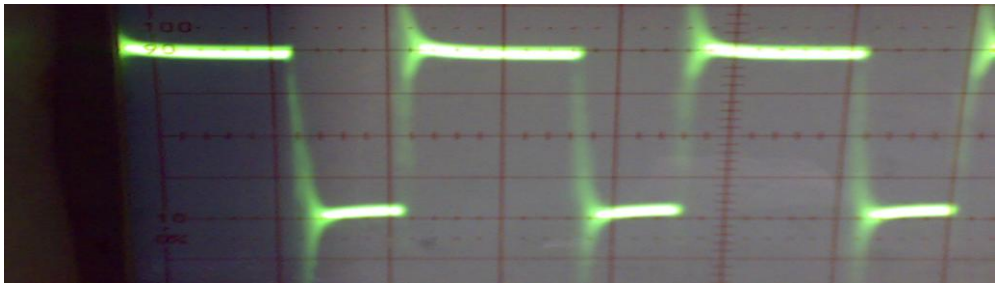


Fig.9.Experimental waveform of the proposed method

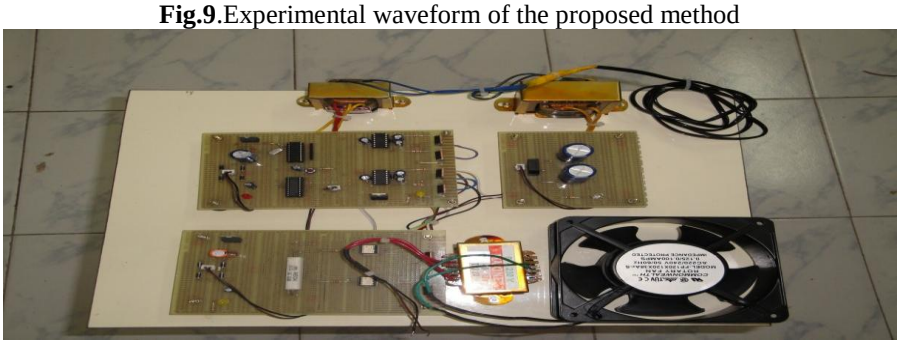


Fig.10. Hardware Setup

The proposed dead elimination circuit is incorporated into a single phase H-Bridge inveter as shown in fig.10. The MOSFET'S used are IRF840.The inverter is loaded with a R-L load resistances of 1KΩ and 100mH. The dc bus voltage is 48V and the frequency of modulation is 50HZ. In addition, the proposed dead-time elimination control scheme can be implemented, contained in the at AT89C2051microcontroller software to reduce hardware cost.

VI. CONCLUSION

In the present work, a novel method for the elimination of dead time in two level voltage source inverter is proposed and implemented. This method reduces the low frequency distortion and results in a steady fundamental voltage. The validity of this method has been studied by the PSPICE Simulation and prototype experiment. Compared to the conventional method , this method has simple control logic, low cost and flexible implementation.

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