International Journal of Engineering Research and Development
e-ISSN: 2278-067X, **p**-ISSN: 2278-800X, www.ijerd.com
Volume 6, Issue 5 (March 2013), PP. 21-29

Harmonic Mitigation Using a Novel Two-Stage Boost Rectifier

M.Prathyusha[1], M.M Irfan[2],Dr.C.Venkatesh[3]
[1]M.Tech Student, SR Engineering College,AP.
[2]Assistant Professor, SR Engineering College, AP.
[3]Associate Professor, SR Engineering College, AP.

Abstract:- Usually high DC output voltage is obtained by circuits such as voltage doubler rectifiers or a diode pump circuits. Even though the circuit configuration of these circuits is simple but, the AC input current contains harmonics. These harmonics can be eliminated by using single phase two stage boost rectifier with single active power device. By using this topology we can reduce the harmonics to a large extent but, input current waveform is distorted and is out of the sinusoidal wave near a zero crossing. In order to overcome the above drawback, a new topology termed as single-phase two stage boost rectifier with two active power devices is proposed. With the proposed topology, output obtained is more than twice the peak input voltage along with sinusoidal input current. The THD is also reduced compared to the previous topology. In both topologies almost unity power factor is maintained. The two topologies are studied, analyzed and simulation models are developed for two circuits using MATLAB software. The simulated results show that the proposed topology has reached the expected performance.

Keywords:- Boost rectifier, THD, Two Stage Rectifier, Current mode control.

I. INTRODUCTION

To obtain higher DC output voltage, voltage-doubler rectifiers which are a half-bridge circuit or a diode pump circuit have been used[1-4] . Although the circuit configuration ofthese rectifiers is simple, the AC input current has thedistorted waveform. The input current contained harmonics. For the purpose of the improved waveform in the inputcurrent by using new configuration of the rectifier without the transformer, the single-phase switch-mode rectifier with cascade connection of the diode bridge and the boost DC–DC converter has been shown[15]. However, the efficiency of the converter decreases rapidly at high duty cycle in the range of high DC output voltage. To maintain high efficiency in the wide operational range, a single-phaseboost rectifier adding a capacitor for pumping action in DC circuit[16]has been proposed by the authors enables the DC output voltage to be regulated and the input current to be close to sinusoidal. However, the input current waveform is degraded as the output power increases. In this paper, a novel single-phase two-stage boost rectifier without the transformer is proposed and a reduction in the input current distortion is studied. Additional capacitor in DC side gives two-stage boost operation by means of inductive and capacitive energy/transfer mechanisms under the high-frequency switching. To cause the input current to follow its sinusoidal reference by employing current mode control, a capacitor voltage is superimposed upon the supply voltage when the switches are turned on. The previous and proposed rectifier have been simulated.The rectifiers of two types, the switching signals, and the control block diagram are shown. The modes of operations are explained by illustrating the equivalent circuits of each mode. The total harmonic distortion (THD) and the efficiencies are compared in two rectifiers. The simulated results confirm that the input current can be wave-shaped sinusoidally with a near unity power factor independent ofthe working conditions

II. SINGLE PHASE TWO STAGE BOOST RECTIFIER WITH SINGLE SWITCH

Fig .1.gives the original topology of the single-phase twostage boost rectifier with single switch[16]which has been reported previously by the authors. This topology is based on the combination of a conventional single-phase boost rectifier and the pump circuit. The boost rectifier, which is first stage for the boost, comprises four diodes labeled D_1–D_4, an active power device IGBT labeled Q, the boost inductor L_1 and the capacitor C_1. The capacitor C_2 for thepumping action, which functions as second stage for theboost is connected in DC side. In the first stage, theenergy is transferred from AC source to the capacitor C_1.

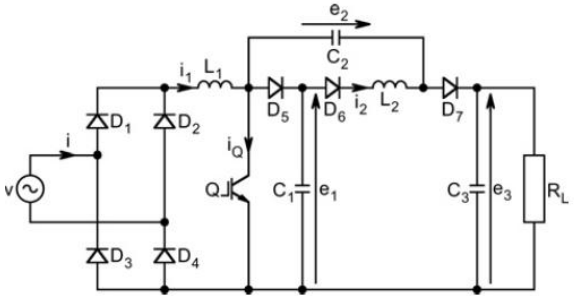


Fig.1 Single-phasetwo-stage boost rectifier with single switch

In the second stage, the energy stored in C_1 is transferred to the capacitor C_2. The pumping action of the capacitor C_2 allows the output capacitor C_3 to produce more than the sum of the peak input voltage and the capacitor C_2 voltage, because C_2 is connected in series to the input source. The inductor L_2 is inserted to suppress the circulated current between the capacitors C_1 and C_2 in the on-state of Q. The diode D_5 is inserted to prevent the capacitor C_1 from being shorted when Q is turned on. The diode D_6 prevents the current i_1 from charging C_1 through L_1, C_2 and L_2 after the current i_2 has reached to zero. The diode D_7 prevents the capacitor C_3 from discharging via C_2 while Q is conducting. In this topology, the input current can almost be wave-shaped sinusoidally by employing a current-mode control. However, the rate of the increase in the input current during the conduction of Q depends on the supply voltage and the boost inductor L_1. The low instantaneous supply voltage in the vicinity of a zero crossing cannot allow the actual current to follow the reference, so that the current waveform is distorted and is out of the sinusoidal wave near a zero crossing. The distortion in the input current becomes serious according to an increase of the load

III. SINGLE PHASE TWO STAGE BOOST RECTIFIER WITH TWO SWITCHES

Fig.2.shows the proposed single-phase two-stage boost rectifier for the purpose of the achievement of the sinusoidal input current without the distortion near the zero crossing of the supply using current mode control. The diode bridge and the pump circuits also are employed for the construction of the topology. Comparing with previous rectifier[16] an active power device and a diode are added. The energy transfer in the proposed topology is the same as that in previous rectifier, and the DC output voltage more than twice the peak input voltage can be obtained. In this topology, the voltage of the capacitor C_1 can be used for the increase of the input current. Then the actual input current can go to the reference with faster response, even if the instantaneous supply voltage is low. Consequently, the distortion of the input current waveform in the vicinity of a zero crossing of the supply is reduced. The detail of the operation is described in the later section. The diodes D_5 and D_6 are inserted to prevent the capacitor C_1 from being shorted when Q_1 and Q_2 are turned

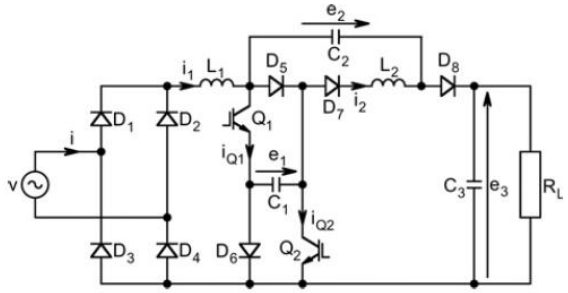
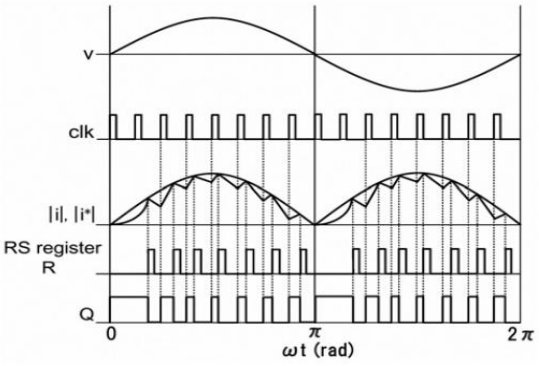


Fig .2. Proposed single-phase two-stage boost rectifier with two switches

A.Switching and control strategies of previous and proposed rectifier

The basis of the boost rectifier with the current-mode controlis as follows[16] the active power device is turned on at thebeginning of the fixed interval, and it is turned off whenthe actual input current reaches the reference. The typical waveforms of the device signals and the inputcurrent are illustrated in fig3for rectifier in fig 1andfig 4for the proposed two-switch rectifierof Fig.2. The device Q within the single-switch rectifiercorresponds to Q_1 within the two-switch rectifier. They areturned on by the clock pulse with the fixed frequency. The input current increases while the device conducts. The device is turned off by the reset signal when theinstantaneous value of the input current is equal to that ofthe reference. The current decreases during the off-state ofthe device. In the two-switch rectifier, the active device $Q_2$is turned on to achieve the fast response with increasinginput current. The conduction of this device allows thevoltage of the capacitor C_1 to

contribute increasing theslope of the current. In the unity power factor condition, since the magnitude of the input current increases graduallyduring $0 < \omega t < \frac{\pi}{2}$and $\pi < \omega t < 3\pi/2$, the on-gatesignals, which are identical with those of Q_1, are applied toQ_2 during these interval



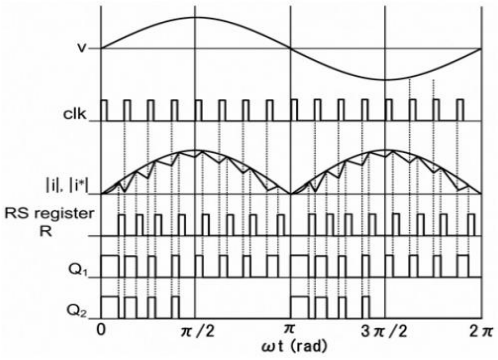


Fig.3. Device signals for single-switch rectifier**Fig. 4**. Device signals for two-switch rectifier

Fig. 5illustrates the control block diagram for the proposed Rectifier and previous rectifier as well [16]. The feedback loop consists of the regulation of the DC output voltage and thegeneration of the sinusoidal input current. The control loopof the voltage mode compares the detected output voltage $e_3$against the command $e_3{}^*$ and adjusts the input current tonegate the voltage error. This is done by a proportionalplus-integral (PI) controller. The computation of the PIalgorithm is executed by a microcomputer in the test setupwhen the interrupt (INT) signal is provided by a phase locked loop at zero crossing every half-cycle of the supply. The output labeled u of the PI controller determines theamplitude of the current reference and it is discretelyregulated with zero-order hold at every interruption. On theother hand, the control loop of the current mode containsthe comparator and the RS register. The sensedinstantaneous value i of the input current is converted intothe absolute value $|i|$, which is one of the two inputs to thecomparator. A read only memory (ROM) contains thedigital data of a full-wave rectified sinusoidal signal withunity amplitude. A digital-to-analogue (D/A) converterchanges the output of ROM into the continuous signal,which is kept in phase with the supply voltage. Thereference $|i^*|$ of the input current is provided from themultiplier and it is given as a product of the signal u and theD/A converter output. The reference is the second input tothe comparator. The switching timings of the two IGBTs labeled Q_1 and Q_2 are determined by the RS register with20 kHz clock that is fixed as the switching frequency ofIGBTs. The output Q of the RS register is set to the highlevel every clock cycle, and it is sent to the device Q_1. Theturn-on of this IGBT causes the actual input current $|i|$ to increase.

If $|i| < |i^*|$, the output of the comparator remainslow and the IGBT is in the on-state. When the current $|i|$reaches$|i^*|$, the output of the comparator changes to thehigh level and so the output Q becomes low. This causes theIGBT to be turned off. The off-state of the IGBT allowsthe input current to decrease and it continues till the nextclock pulse is provided to the RS register again. As shown in Fig. 4, the on-gate signal with the duration$\pi/2$ is applied to the device Q_2. This signal is generated bya monostable. The monostables 1and 2 are triggered bythe zero cross signal with the positive slope and thenegative slope of the supply voltage, respectively. Theoutputs of two monostables are sent to logic OR. This provides continuously the on-gate signal to Q_2 during$0 < \omega t < \pi/2$and $< \omega t < 3\pi/2$. The control scheme inthis section can guarantee that the sinusoidal input currentis maintained with a near unity power factor even if theload is varied.

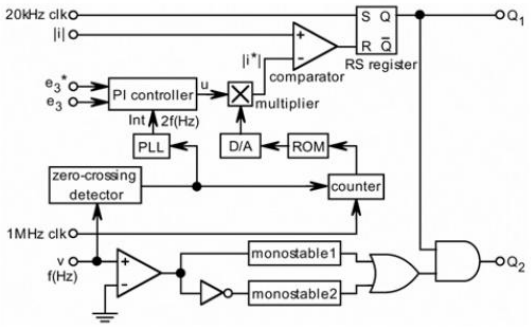


Fig. 5. Control block diagram

B. Modes of operation:

In the single-phase rectifier, the operations during the positivehalf-cycle of the supply are the same as those during the negativehalf-cycle of the supply, and the input current can besymmetrically wave-shaped. Then the operation of theproposed two-switch boost rectifier during the interval0 $<\omega t<\pi$ shown in Fig. 4is considered. The processrepeats with the input current increasing in the on-state ofthe active power device and decreasing in the off-state. This section gives the equivalent circuits and explainsthe operation in each mode during one switching cycle ofthe active power device, assuming the boost conditions$|v|<e_1$, $|v|<e_3$_$-e_2$ with the discontinuous i_2. Thesingle-switch rectifier has the same mode of the operation asthe two-switch rectifier, except that the device Q_2 conducts.

Modes 1 and 2:

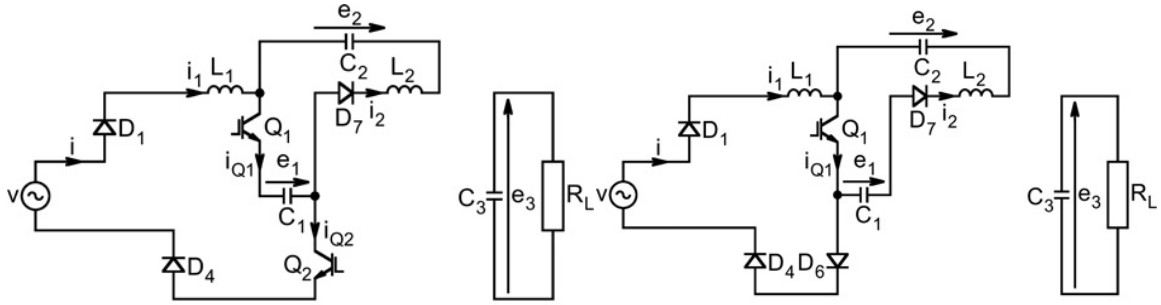


Fig.6.a)Mode 1 (Q_1=on,Q_2 = on, $i_1\geq 0$) b) **Mode 2** (Q_1=on ,Q_2 = off, $i_1\geq 0$)

When the devices Q_1 and Q_2 are turned on, in the interval$0<\omega t<\pi/2$, the circuit operation of mode 1 shown inFig. 6 astarts. In the interval$\frac{\pi}{2}<\omega t<\pi$, only Q_1 isturned on and this mode of the operation is shown asmode 2 in Fig.6b. In both modes, although the inputcurrent i_1 increases and the energy is stored in the boostinductor L_1, the response of the current differs betweenthese modes. The current i_1 in mode 1 flows through thefollowing loop

$$v–D_1–L_1–Q_1–C_1–Q_2–D_4$$

that in mode 2 flows through

$$v–D_1–L_1–Q_1–D_6–D_4$$

The increase of the input current in mode 1 is caused by thecapacitor voltage e_1 that is superimposed on the supplyvoltage, while the increasing current response in mode 2depends upon the supply voltage only. The input currentincreases at a rate proportional to $(|v|+e_1)/L_1$ and $|v|/L_1$in modes 1 and 2, respectively. In results, the input currentincreasing in mode 1 will have faster response than that inmode 2. The single-switch rectifier contains mode 2 onlyin the operation. The two-switch rectifier has the improvedcurrent waveform at the low instantaneous supply voltage, compared with that of the single-switch rectifier. On theother hand, in both modes, the current i_2 that equals toi$_{Q1}$- i$_{Q2}$ flow through the following loop

$$C_1–D_7–L_2–C_2–Q_1$$

And it increase at a rate proportional to (e_1- e_2)/L_2. Thecapacitor C_1 is discharged and C_2 is charged. As the energystored in C_1 is transferred to C_2, the voltage e_1 willdecrease and e_2 will increase slightly. In these modes, thediode D_8 is reverse-biased and the load with C_3 is isolatedfrom the supply. The energy stored in the output capacitorC_3 is supplied to the load and then the voltage across thecapacitor C_3 will decrease slightly. The device Q_1 is turned off when the actual input current i in mode 1 or 2 reaches the reference. In mode 1, Q_2 also isturned off simultaneously.

Modes 3 and 4**:**

The mode 3 or 4 shown inFig.7comes after mode 1 or 2, if the current i_2 is notzero. The mode of the operation depends on therelationship of the capacitor voltages e_1, e_2 and e_3. In thecondition of e_1+e_2< e_3, the diode D_6 is in the on-stateand D_8 is reverse biased. The current path of mode 3shown in Fig. 7 ais formed in the rectifier. The inputcurrent i_1 flows through

$$v–D_1–L_1–D_5–C_1–D_6–D_4$$

and the capacitor C_1 is charged. The current $i_2$circulatesthrough

$$L_2–C_2–D_5–D_7$$

And it decreases with charging the capacitor C_2. On the otherhand, in the condition of $e_1 + e_2 > e_3$, the diode D_6 is blockedand D_8 is conducting. When $i_1 > i_2$, the current i_1 flowsthrough two paths, that is C_2 and D_5–D_7–L_2, as shown inFig. 7 b. The capacitor C_2 is discharged and C_3 is charged. If$i_1 < i_2$, the current i_1 flows through D_5–D_7–L_2–D_8, withcharging C_3. The circulated current of i_2-i_1 flows in theloop L_2–C_2–D_5–D_7. The capacitor C_2 is charged. In bothmodes, the input current i_1 decreases

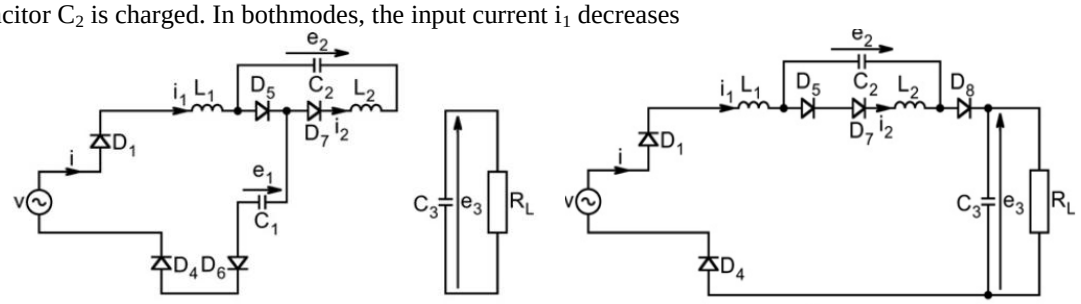


Fig7 a) Mode 3 ($e_1 + e_2 < e_3$), $i_2 > 0$, $Q_1 = Q_2$= off **b)** Mode 4 ($e_1 + e_2 > e_3$) , $i_2 > 0$,$Q_1 = Q_2$=off

Modes 5,6,7,8:

When the current i_2 is reduced to zero, in mode 3 or 4, therectifier is in any mode of the operations shown in Fig. 8Modes 5–7 of the operations have a non-zero current of i_1.In mode 5 with the condition of $e_1 + e_2 < e_3$, the diode $D_6$is in conducting and D_8 is reverse biased. The current $i_1$flows through the following loop

$$v–D_1–L_1–D_5–C_1–D_6–D_4$$

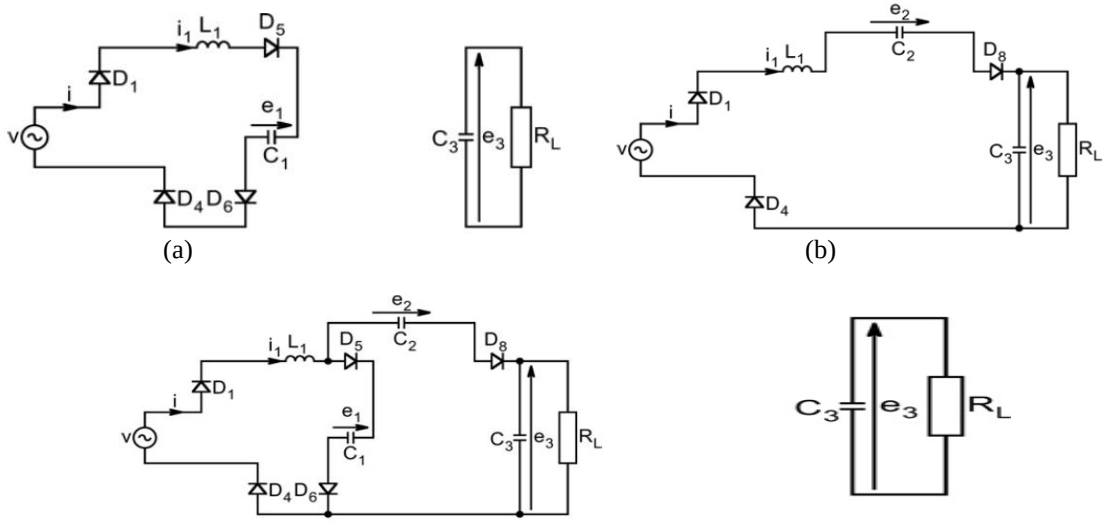
and the capacitor C_1 is charged. The energy stored in theoutput capacitor C_3 is supplied to the load.

If $e_1 + e_2 > e_3$, the diode D_6 is blocked and D_8 is in the on-state, as mode 6 shown in Fig. 8 b. The current i_1 flows into the load with the capacitor C_3, through the capacitor C_2. Then the capacitors C_2 and C_3 are discharged and charged, respectively When $e_1 + e_2 = e_3$, the rectifier is in mode 7 of the operation shown in Fig. 8 c. In this mode, both the diodes D_6 and D_8 are in conducting. The current i_1 flows through two paths

$$v–D_1–L_1–D_5–C_1–D_6–D_4$$

And

$$v–D_1–L_1–C_2–D_8–C_3/R_L–D_4$$



(a) (b)

(c) (d)

Fig. 8a)Mode 5 ($e_1 + e_2 < e_3$, $i_1 > 0$) with $i_2 = 0$ in off states of Q_1 and Q_2

b) Mode 6 ($e_1 + e_2 > e_3$, $i_1 > 0$) with $i_2 = 0$ in off states of Q_1 and Q_2

c) Mode 7 ($e_1 + e_2 = e_3$, $i_1 > 0$) with $i_2 = 0$ in off states of Q_1 and Q_2

d)Mode 8 ($i_1 = 0$,$i_2 = 0$)

The capacitors C_1 and C_3 are charged, and C_2 is discharged. Inthesemodes decreasing the input current i_1, if the energy storedin the boost inductor L_1 is completely discharged and so thecurrent i_1 is reduced to zero, mode 8 shown in Fig. 8dcomes. In this mode of the operation, all the devices stop conducting. This mode exists in the very short interval near the zerocrossing of the supply. The sequence of mode during theinterval with the off-state of the active power devices dependson the capacitor voltages and the load condition

IV. SIMULATION RESULTS

In the simulation environment, the operating conditions and the circuit constants are set as follows:

V= 50 V(rms value of supply voltage)

f = 60 Hz

L_1= 2.10mH (R_1 = 0.108 Ω)

L_2= 13.8μH (R_2 =4.40 Ω)

$C_1 = C_2$ = 1000 μF

C_3= 2200μF and R_L = 62.5 Ω.

The switching frequency is fs = 20 kHz corresponding to the clock frequency for the RS register. The mean value E_3 of the output voltage e_3 is set to 150 V,which is a little higher than twice the peak value of the supply.

A. Simulation model of single phase two stage boost rectifier with single switch

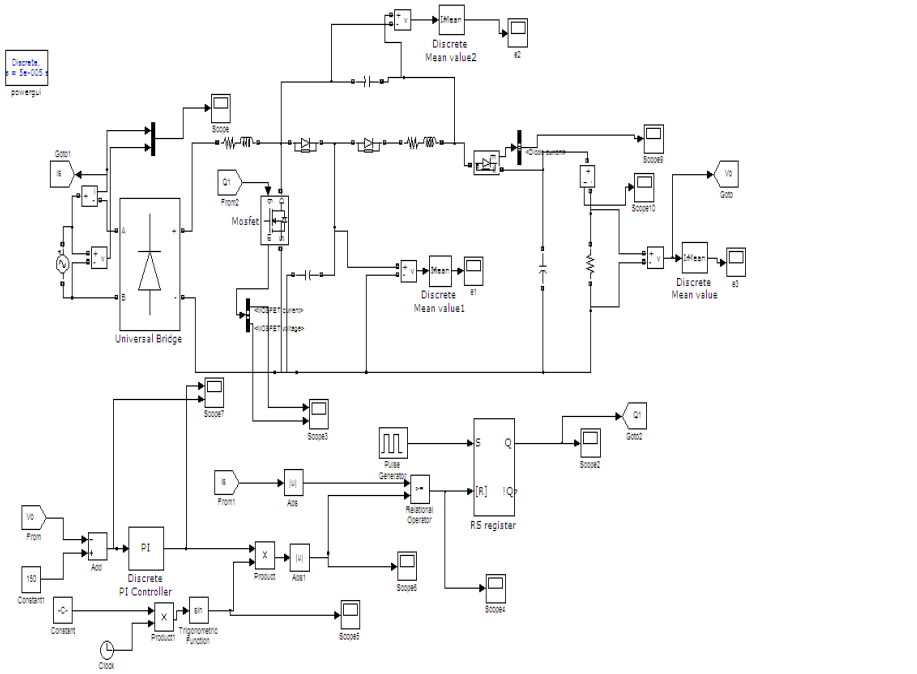


Fig . 9.simulation model of single phase boost rectifier with single switch

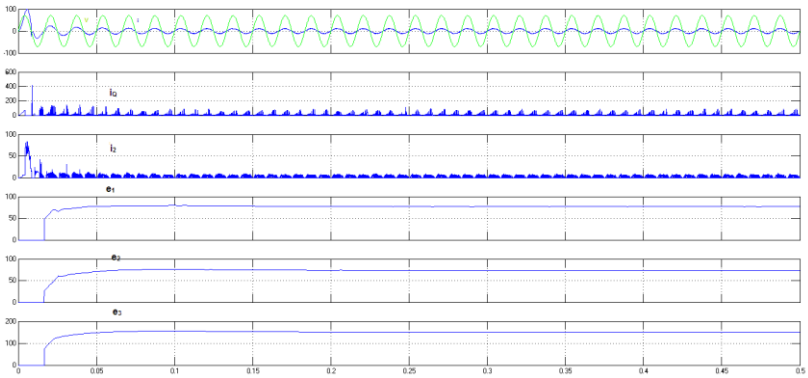


Fig .10.simulation waveforms of single phase boost rectifier with single switch

B. Simulation model of single phase two stage boost rectifier with two switches

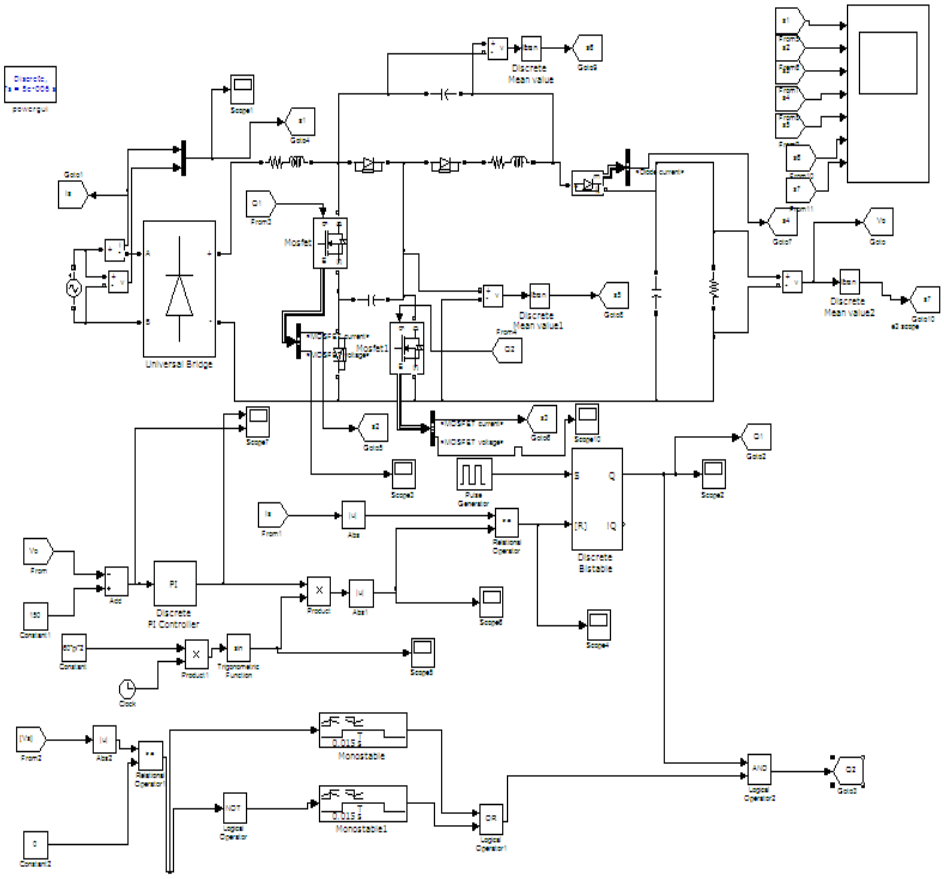


Fig . 11. simulation model of single phase boost rectifier with two switches

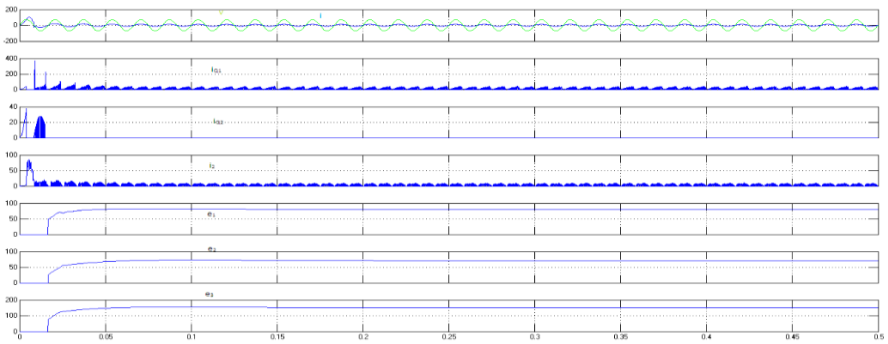


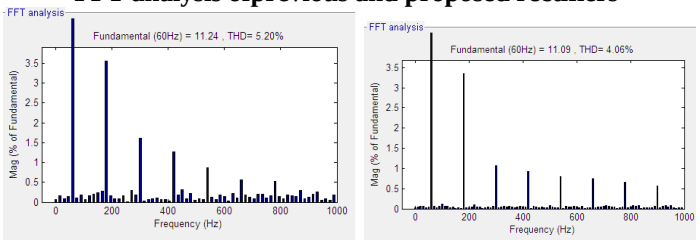
Fig .12.simulation waveforms of single phase boost rectifier with two switches

From the waveforms, it is observed that the input current i can be sinusoid ally wave-shaped without the distortion in the vicinity of a zero crossing of the supply and it is in phase with the supply voltage. The existenceof mode 1 of the operation in the proposed rectifier contributes towards the achievement of the sinusoidal current. In the device Q_2,the current i flows through it during the conduction. On the other hand, the current i_{Q1} through Q_1 is similar to the current i_Q of Fig. 10in the waveform and the waveforms of the voltages across capacitors are identical with those in Fig. 10. This means that the circuit parameters of the proposed rectifier can have the same values as those of the previous rectifier. In the single-phase system, the voltages of all the capacitors within the rectifier pulsate with twice the supply frequency, because the instantaneous power of the AC supply pulsates. The magnitude of the voltage pulsation in the capacitor becomes larger as the capacitance is smaller. The currents i_{Q1} and i_2 depend on the value of L_2 and the voltages of C_1 and C_2. As the large voltage pulsation with small capacitance causes the current i_2 to become large and may affect the operations of the current mode control for the sinusoidal input current. Although the values of the capacitances

are difficult to be derived theoretically, those used in the simulation guarantee the sinusoidal wave of the current i and the allowable current of the devices in the output range of the experiment

C. THD analysis:

FFT analysis ofprevious and proposed rectifiers



(a) (b)

Fig 13 a)Harmonic analysis of rectifier with single switch i.e previous rectifier
b) Harmonic analysis of rectifier with single switch i.e proposed rectifier

The above analysis show that the THD value for Single phase two stage boost rectifier with single switch is 5.20%and that of proposed is 4.06% .The THD value of proposed is reduced than the previous one.

D. Graphs:

For different values of load we have taken output voltage values,output current ad input current value and calculated the efficiencies.From FFT analyser,we have tabulated the THD values for different loads

Table I.THD and efficiency values at different loads for rectifier with single switch

S.NO	R	E_3 /V(λ)	η	THD
1	62.5	3.1	77%	5.20
2	100	3.2	73%	7.52
3	250	3.26	70.3%	15.69

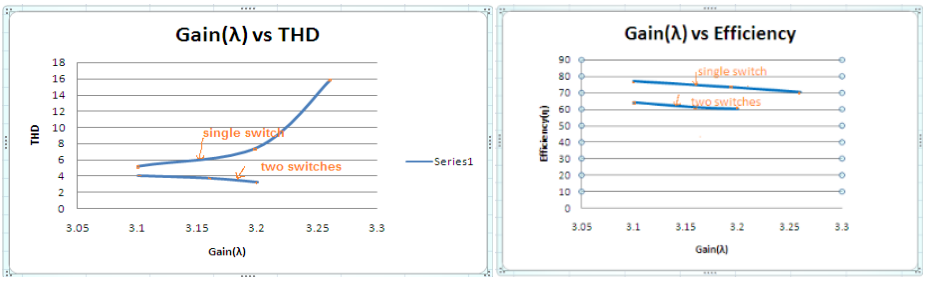
Table II.THD and efficiency values for different loads for rectifier with two switches

S.NO	R	E_3 /V(λ)	η	THD
1	62.5	3.1	64%	4.04
2	80	3.16	61%	3.73
3	100	3.2	60%	3.24

Tables I and IIshows the measured THD factors, the measured efficiencies η in each rectifier when the output voltage is varied. The circuitconstants and the operating conditions are the same in each rectifier. The step-up ratio λ is defined as the ratio of themean output voltage to RMS value of the supply voltage asfollows

$$\lambda = E_3/V$$

In the previous rectifier with single switch, the THD becomes larger rapidly as λ increases. The larger THD is caused by the distortion in the vicinity of a zero crossing of the supply The THD of the proposed rectifier with two switches is reduced to less than 5% and it also decreases as λ increases



(a) (b)

Fig.14. a)Gain (λ) vs THD graph for previous and proposed rectifiers
b)Gain (λ) vs Efficiency graph for previous and proposed rectifiers

The THD of the proposed rectifier with two switches is reduced to less than 5% and it also decreases as λ increases. The reduced THD of the proposed rectifier is due to forcing the input current to follow its sinusoidal reference, by discharging the capacitor via two active power devices. This means that the proposed rectifier can always draw a sinusoidal input current from the supply over the wide range of the output voltage. On the other hand, the efficiency of the proposed rectifier is a little lower than that of the previous rectifier, because of the addition of the active power device and diode. It seems that the major source of the power loss is the conduction loss because of the power device forward voltage drops. However, these power devices are intrinsically required to improve the input current waveform. The measured values of the input power factor are nearly equal to the unity in both two rectifiers.

V.CONCLUSION

The proposed topology and the previous topology has been studied,analyzed and simulated.From the simulation results, we observe that proposed rectifier has high output voltage i.e. more than the twice the peak input voltage along with sinusoidal input current and input contains reduced harmonics than the previous rectifier. The power factor of both the circuits is maintained at almost unity .We have performed the FFT analysis on both the circuits,FFT analysis proves that proposed rectifier has less THD (4.04%) compared to the previous one with THD(5.20%). The relative current, voltage values for different load values have been tabulated and efficiencies have been calculated. From the tabulated values, graphs have been drawn for Gain vs. efficiency for both rectifiers, and also for Gain vs. THD.It has been seen that for the proposed rectifier, the THD is kept small over the wide range of the output voltage. We also observe that efficiency will decrease slightly for proposed rectifier due to the use of many devices.We can conclude that the proposed rectifier is best suited for obtaining high dc output voltage and reduced harmonic distortion at ac input mains even at zero crossing.

REFERENCES

[1]. BOYS J.T., GREEN A.W.: 'Current-forced single-phase reversible rectifier', IEE Proc., Electr. Power Appl., 1989,136, (5), pp. 205–211

[2]. SALMON J.C.: 'Circuit topologies for single-phase voltage doubler boost rectifiers', IEEE Trans. Power Electron., 1993,8, (4), pp. 521–529

[3]. MAZDA F.F.: 'Power electronics handbook' (Butterworths,1990)

[4]. SINGH B., SINGH B.N., CHANDRA A., AL-HADDAD K., PANDEY A.,KOTHARI D.P.: 'A review of single-phase improved powerquality AC–DC converters', IEEE Trans. Ind. Electr., 2003,50, (5), pp. 962–981

[5]. J. C. Salmon, "Techniques for minimizing the input current distortion of current-controlled single-phase boost rectifiers," *IEEE Trans. PowerElectron.*, vol. 8, pp. 509-520, Oct. 1993.

[6]. QIAN J., ZHAO Q., LEE F.C.: 'Single-stage single-switch powerfactor correction AC/DC converters with dc-bus voltagefeedback for universal line application', IEEE Trans. PowerElectron., 1998, 13,(6), pp.1079–1088

[7]. DANIELE M., JAIN P.K., JOOS G.: 'A single-stage power-factorcorrectedAC/DC converter', IEEE Trans. Power Electron.,1999, 14, (6), pp. 1046–1053

[8]. CHOW M.H.L., LEE Y.S., TSE C.K.: 'Single-stage single-switchisolated PFC regulator with unity power factor, fasttransient response, and low-voltage stress', IEEE Trans.Power Electron., 2000, 15, (1), pp. 156–163

[9]. H. O. Aintablian and H. W. Hill, "A new single phase ac to dc harmonic reduction converter based on the voltage-doubler circuit," in *Proc. IEEEIECON'94*, 1994, pp. 452-457.

[10]. WEI H., BATARSEH I., ZHU G., KORNETZKY P.: 'A single-switch ac–dc converter with power factor correction', IEEE Trans.Power Electron., 2000, 15, (3), pp. 421–430

[11]. QIAO C., SMEDLEY K.M.: 'A topology survey of single-stagepower factor corrector with a boost type input current shaper', IEEE Trans. Power Electron., 2001, 16, (3),pp. 360–368

[12]. LU D.D.C., CHENG D.K.W., LEE Y.S.: 'Single-stage AC–DCpower-factor-corrected voltage regulator with reducedintermediate bus voltage stress', IEE Proc. – Electr.. PowerAppl., 2003, 150, (5), pp. 506–514

[13]. LIN J.L., CHANG M.Z., YANG S.P.: 'Synthesis and analysis for anovel single-stage isolated high power -factor correction converter', IEEE Trans. Circuit Syst. I, 2005, 52, (9),

[14]. LU D.D.C., IU H.H.C., PJEVALICA V.: 'A single-stage ac/dcconverter with high power factor, regulated bus voltage, and output voltage', IEEE Trans. Power Electron., 2008,23, (1), pp. 2274–2286

[15]. TAKAHASHI I., IKESHITA W.: 'Improvement of input currentwaveform of a single-phase rectifier circuit', Trans. IEEJpn, 1985, 105-B, (2), p. 82

[16]. OISHI H., NEBA Y., ISHIZAKA K., ISHIZAKA R.: 'Single-phaseboost rectifier adding a capacitor for pumping action in DCcircuit', Trans. IEE Jpn, 2007, 127-D, (3), pp. 347–348