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Comparative Logic Styles In Design Of Adder Using VLSI

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Abstract:- The main consideration for design and implementation a doubly-fed induction generator (DFIG) applied to wind power generation driven by wind turbine is under study for low voltage ride-through application during system unbalance. An improved control and operation of DFIG system under unbalanced grid voltage conditions by coordinating the control of both the rotor side converter (RSC) and the grid side converter (GSC) is done in this thesis. Simulation and analysis of DFIG system with wind turbine using Fuzzy logic controller for RSC and GSC under unbalanced condition is presented in the positive synchronous reference frame The steady-state operation of the DFIG and its dynamic response to voltage sag resulting from a remote fault on the 120-kV system is shown in this thesis using controllers. Modeling of DFIG system under Fuzzy logic controller to control voltage and active-reactive powers is done using MATLAB/SIMULINK.

Keywords:- Converter, doubly fed induction generators (DFIGs), proportional integral (PI) plus resonant (R; PI–R), voltage unbalance, wind energy

I. INTRODUCTION

WIND turbines based on doubly fed induction generators(DFIGs), with converters rated at about 25%–30% of The generator rating, have been widely used for large-scalewind generation. DFIG-based system studies have been mainly based on a symmetrical grid voltage supply [1]–[4].design levels, such as architectural, circuit layout, and the process technology level [1-3]. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation, switching capacitance, transition activity, and short-circuit currents are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important, disallowing the formulation of universal rules for optimal logic styles. Power dissipation has become a critical design metric for large number of VLSI circuits. The exploiting market of portable electronic appliances fuels the demand for complex integrated system that can be powered by lightweight batteries with larger recharge time. Therefore, in modern VLSI era the demand of low power design style becomes a hot research topic.

This paper analyzes 16bit carry skip adder using pass-transistor logic styles. These implementations are compared based on transistor count, power dissipation, and delay and power delay product. The power delivered in the output is one of the main factors to analyze the power dissipation of the circuit. The designed adder circuit has reduced the power dissipation due to CPL circuit implantation because it uses n-MOSFET. The propagation delay of our circuit has reduced tremendously than the reported results. The propagation delay, power dissipation and power delay product has obtained for different known sub micron feature size [14].

II. DESIGN METHODOLOGY

A ripple-carry adder is the simplest so that it is easy to design but is only practical for the implementation of additions with a relatively small word length because the linear dependence of the adder speed on the number of bits makes the usage of the ripple-carry adder rather impractical; since the carry bit "ripple" from one stage to the other, the delay through the circuit depends on the number of logic stages that must be traversed and is a function of the applied input signals. Fig1. Shows ripple-carry adder constructed by cascading full adders in series. In ripple carry adder every full adder cell has to wait for the incoming carry before an outgoing carry can be generated [4].

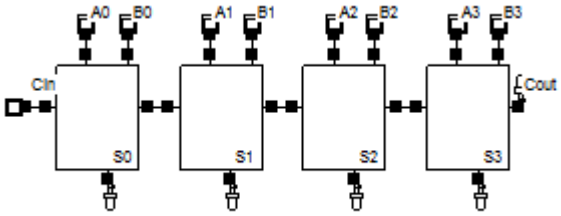


Fig.1: Ripple carry adder

This dependency can be eliminated by introducing an additional bypass (skip) to speed up the operation of the adder. An incoming carry C_{in}=1 propagates through complete adder chain and causes an outgoing carry C_{out}=1 under the conditions that all propagation signals are 1. This information can be used to speed up the operation of the adder, as shown Fig 2. When BP = $P_0P_1P_2P_3$ = 1, the incoming carry is forwarded immediately to the next block through the bypass and if it is not the case, the carry is obtained via the normal route.

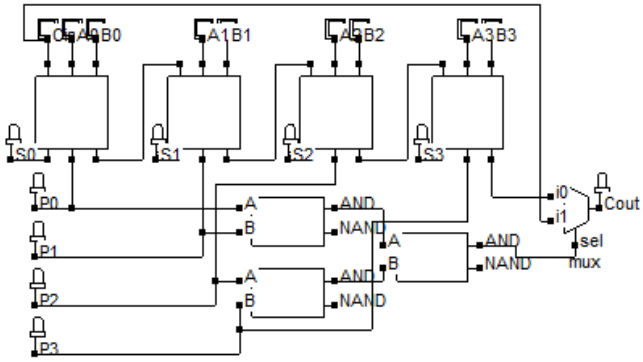


Fig.2: 4-bit Carry skip adder

By cascading four 4 bit carry skip adders in series we can construct 16 bit carry skip adder which is shown in figure In the same way we can construct 32, 64 carry skip adders also.

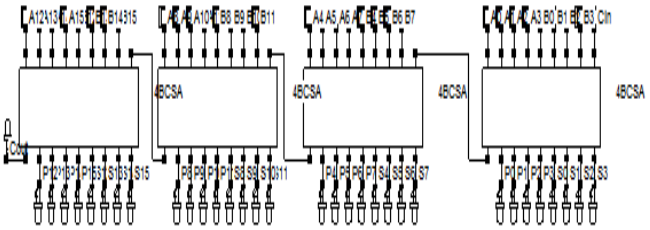


Fig.3: 16 bit Carry skip adder

III. CARRY SKIP MECHANICS

Boolean equations:

From the full adder circuit shown in figure 4.

Carry propagate $Pi=A_i$ XOR B_i,

Sum $Si=P_i$ XOR C_i, and

Carry out $C_{i+1}=A_i B_i + P_i C_i$. From these equations we can observe if $A_i=B_i$ then $p_i=0$, it makes carry out C_{i+1} depends only on Ai and B_i that is $C_{i+1}= A_i B_i$

Carry out C_{i+1}=0 if Ai = B_i = 0

Carry out C_{i+1}=1 if A_i = B_i = 1

If $A_i \neq B_i$ then Pi=1 Carry out C_{i+1} is equal to the input carry C_i. So for all the input combinations which are not equal the outgoing carry C_{i+1} is equal to the input carry C_i.

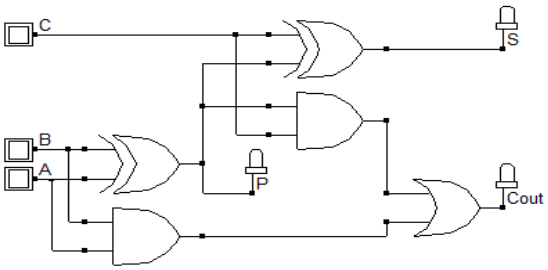


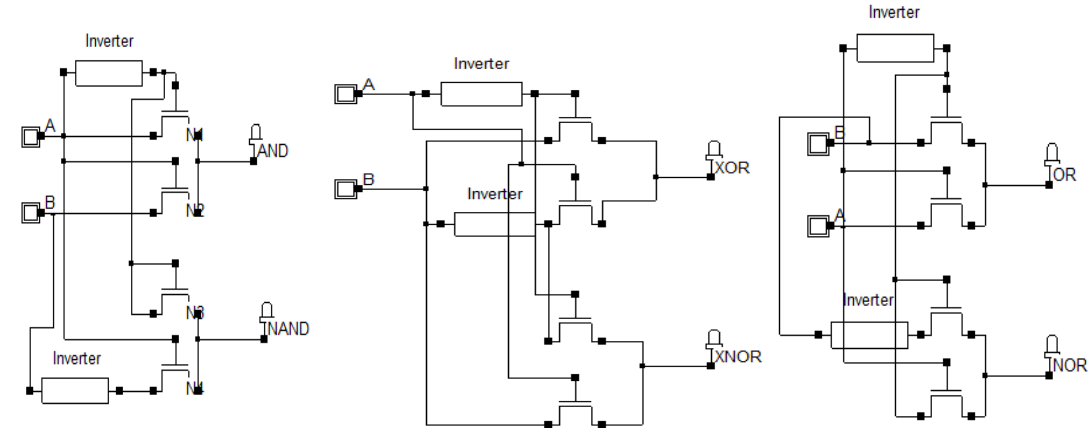
Fig.4: Full adder

A. Non-Clocked Pass gate logics

A logic style is the way how a logic function is constructed from a set of transistors. It influences the speed, size, and power dissipation and wiring complexity of a circuit. All these characteristics may vary considerably from one logic style to another and thus make the proper choice of logic style crucial for circuit performance.

B. Complementary Pass Transistor Logic (CPL)

The full adder circuit designed by using complementary pass transistor logic (CPL) has swing restoration ability. The basic difference between the pass-transistor logic and the complementary CMOS logic styles is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network (either PMOS or NMOS) is sufficient to implement the logic function, which results in smaller number of transistors and input loads especially when NMOS network used. However, pass-transistor logic has an inherent threshold voltage drop problem. The output is a weak logic "1" when logic "1" is passed through a NMOS and a weak logic "0" when logic "0" is passed through a PMOS [2-5, 9]. Therefore, output inverters are also used to ensure the drivability.



(A) AND Gate (B) XOR Gate (C) OR Gate

Fig.5: (A) AND, (B) XOR, (C) OR Gate using Complementary Pass Transistor Logic

C. Differential Cascade Voltage Swing Pass Transistor Logic (DCVSPL)

The DCVS logic with the pass gate is a means of extending the performance benefits associated with DCVSL into pass gate topologies. The performance of DCVSPG logic can be extended by implementing pass gate topology. Static DCVSL is a differential style of logic which requires both true and complementary signals to be routed to gates. Two complementary NFET switching trees are connected to cross-coupled PFET transistors [2-5]. Depending on the differential inputs, one of the outputs is pulled down by the corresponding NFET network. The cross-coupled PFET transistors then latch the differential output. Since the inputs drive only the NFET transistors of the switching trees, the input capacitance is typically two or three times smaller than that of the conventional static CMOS logic[3,10,11].

In DCVSPG, both the NFET and PFET contribute to pull up performance, and both true and complement outputs are actively driven to their logical value. The PFET device sizing sensitivity problem in conventional DCVS is also eliminated. So that improperly sized PFET does not affect functionality. The DCVS logic with the pass gate is a means of extending the performance benefits associated with DCVSL into pass gate topologies. Static DCVSL is a differential style of logic requiring both true and complementary signals to be routed to gates [12-13]. Depending on the differential inputs, one of the outputs is pulled down by the

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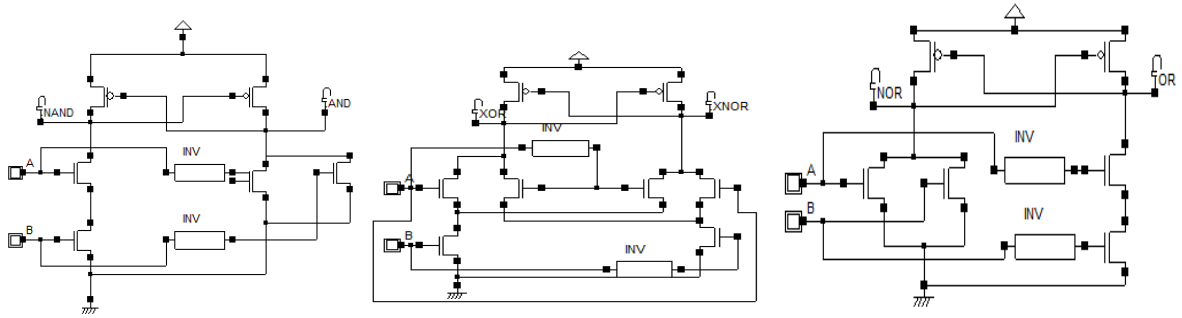
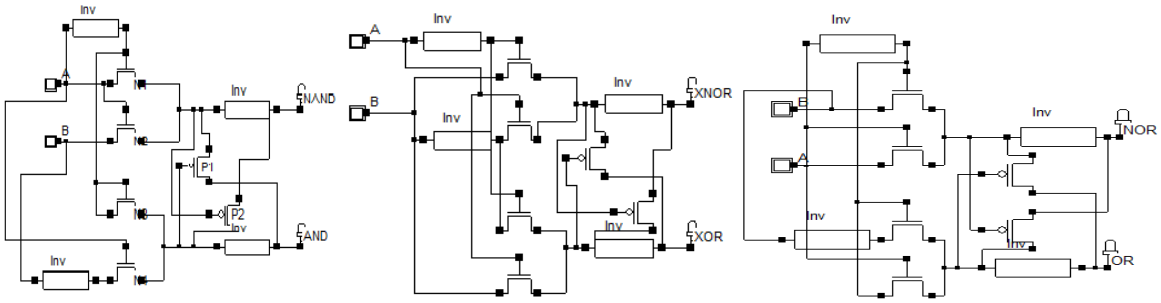


(A) AND Gate (B) XOR Gate (C) OR Gate

Fig.6: (A) AND Gate (B) XOR Gate (C) OR Gate Using Differential cascade voltage swing pass transistor logic

D. Energy Economized Pass Transistor Logic (EEPL)

The improvement to pass gates is to restore full voltage level swing while avoiding the FET horsepower necessary to overcome the hysteresis of the latch [2-5, 10, 11]. EEPL reduces power Consumption and delay by interrupting the feedback of the latches forming the load circuit in the Structure, allowing reduction in the width of the NFET devices comprising the evaluate tree. The Device width reduction further contributes to the power reduction. The circuit action simultaneously provides regenerative positive feedback, providing shorter delays than comparative CPL circuits. EEPL will be a valuable logic element in low power applications where performance is still essential.

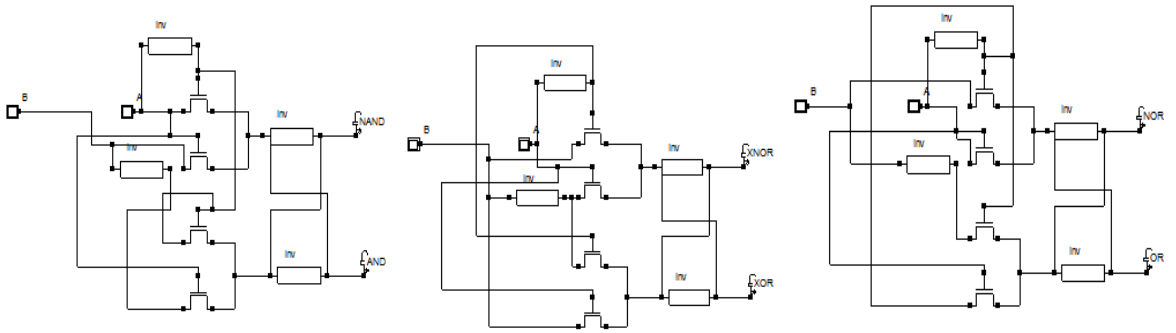


(A) AND Gate (B) XOR Gate (C) OR Gate

Fig.7: (A) And Gate (B) XOR Gate (C) OR Gate Using Energy economized pass transistor logic (EEPL)

E. Swing Restored Pass Gate Logic (SRPL)

The generic SRPL gate consists of two main parts as shown in fig8. A complementary output pass transistor logic network that is constructed of n-channel devices and latch type swing restoration circuit consisting of two cross coupled CMOS inverters. The gate inputs are of two types: Pass variables that are connected to the drains of the logic network transistors and control variables that are connected to the gates of the transistors. The logic network has the ability to implement any random Boolean logic function. The complementary outputs of the pass transistor logic network are restored to full swing by the swing restoration circuit [1].



(A) AND Gate (B) XOR Gate (C) OR Gate

Fig.8: (A) And Gate (B) XOR Gate (C) OR Gate using Swing restored pass gate logic

IV. RESULTS

16 bit Carry skip adder has implemented in different pass transistor techniques and is simulated using

CAD tools DSCH3 and microwind3.1 in submicron in regime. All the schematics were drawn using 65nm technology with a 1 V supply voltage. The calculation of power, delay, power delay product and area were carried out for 16 bit carry skip adder in CPL, DCVSPG, EEPL, SRPL logic style and the values are shown in Table 1.

Table I: Performance of 16 bit carry skip adder in all the logic styles for 65nm technology.

Logic style	Power consumption (mw)	Delay (ns)	Power delay product	Area (μm^2)
CPL	0.555	0.448	$0.224x10^{-12}$	9537
DCVSG	0.787	0.807	$0.635x10^{-12}$	11429
SRPL	4.550	1.186	$5.396x10^{-12}$	16601
EEPL	5.512	1.520	$8.378x10^{-12}$	19390

Table II: Performance of 16 bit carry skip adder in all the logic styles for 90 nm technology.

Logic style	Power consumption(mw)	Delay (ns)	Power delay product	Area (μm^2)
CPL	1.245	1.040	$1.294x10^{-12}$	15742
DCVSPG	1.896	1.840	$3.488x10^{-12}$	18854
SRPL	14.766	2.700	$39.86x10^{-12}$	27534
EEPL	18.623	3.445	$64.15x10^{-12}$	31629

The graphs below shows power, delay, area, power delay product for different logics in 65nm technology.

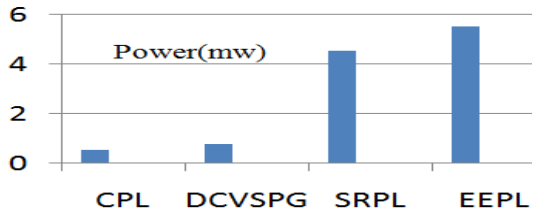


Fig.9: Logic styles Vs Power dissipation for 16 bit carry skip adder

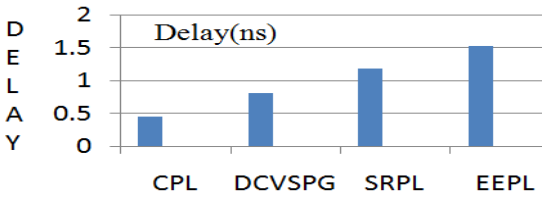


Fig.10: Logic styles Vs Delay for 16 bit carry skip adder

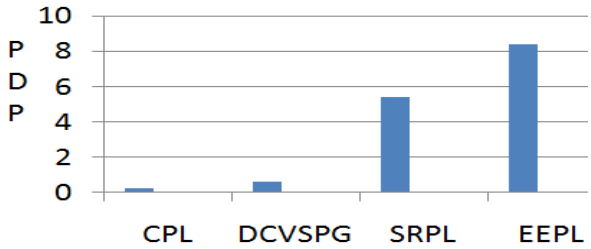


Fig.11: Logic styles Vs PDP for 16 bit carry skip adder

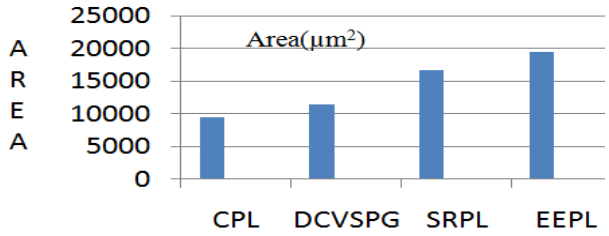


Fig.12: Logic styles Vs Area for 16 bit carry skip adder

V. CONCLUSIONS

This paper analyzes power-dissipation, propagation delay, power delay product of 16 bit adder circuit using different types of pass gate such as CPL, DCVSPG, SRPL, EEPL logic styles. It is found that the CPL adder circuit is faster and gives better performance in terms of power consumption, propagation delay, power delay product.

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