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Continuous Conduction Mode of Bridgeless SEPIC Power Factor Correction Rectifier

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Abstract:- This paper deals with modelling and simulation of Single phase AC-DC Bridgeless Continuous Conduction Mode (CCM) with Single Ended Primary Inductance Converter (SEPIC) for Power Factor Correction (PFC) rectifier. The topology is improved by the absence of an input diode bridge and the presence of only two semiconductor switches in the current flowing path during each switching cycle which results in lesser conduction losses and improved thermal management compared to the conventional SEPIC converters. By implementing the improved topology in CCM it ensures almost unity power factor in a simple and effective manner. The CCM operation reduces the complexity of the control circuitry. An operating principle and a detailed analysis of the proposed converter are presented. It is shown that the efficiency of the SEPIC Converter can be significantly improved. Performance Comparisons between the improved and conventional SEPIC PFC rectifier are carried out using MATLAB software and result is presented.

Keywords:- Continuous Conduction Mode (CCM), Single Ended Primary Inductance Converter (SEPIC), Power Factor Correction (PFC).

I. INTRODUCTION

SEPIC is a DC/DC converter topology that provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. This type of conversion is handy when the designer uses voltages from an unregulated input power supply. Hence this is very much preferred in applications such as battery chargers, power electronic circuits, home appliances, aircraft due to its less electromagnetic interference, inherent inrush current, reduced noise disturbances and less switching losses.

Fig. 1 shows an example of a conventional PFC Sepic rectifier. Referring to Fig. 1, it is clear that the current path flows through rectifier bridge diodes and the power switch (Q) during the switch on-time, and two rectifier bridge diodes and the output diode (D_0) during the switch off-state. Thus, during each switching cycle, the current flows through three power semiconductor switches. This approach is suitable for a low power range. In the low-line input and high-power applications, the high conduction loss caused by the high forward voltage drop of the bridge diode begins to degrade the overall system efficiency, and the heat generated within the bridge rectifier may destroy the individual diodes.

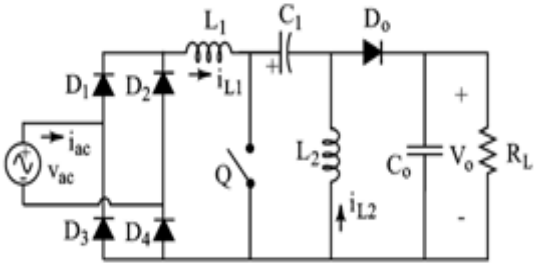

Fig 1: Conventional SEPIC PFC Rectifier

Most of the presented bridgeless topologies so far [1]–[9] implement a boost-type circuit configuration (also referred to as dual-boost PFC rectifiers) because of its low cost and its high performance in terms of efficiency, power factor, and simplicity. These features have led power supply companies to start looking for bridgeless PFC circuit topologies. In [7], a systematic review of the bridgeless PFC boost rectifier implementations that have received the most attention is presented along with their performance comparison with the conventional PFC boost rectifier. The bridgeless boost rectifier has the same major practical drawbacks as the conventional boost converter, such that the dc output voltage is always higher than the peak input voltage, input–output isolation cannot easily be implemented, the startup inrush current is high, and there is a lack of current limiting during overload conditions. Moreover, it is well known that the boost converter operating in discontinuous current mode (DCM) can offer a number of advantages such as inherent PFC function, very

simple control, soft turn-on of the main switch, and reduced diode reversed-recovery losses. However, the DCM operation requires a high-quality boost inductor since it must switch extremely high peak ripple currents and voltages. As a result, a more robust input filter must be employed to suppress the high-frequency components of the pulsating input current, which increases the overall weight and cost of the rectifier.

The main features of the presented converter include high efficiency, low voltage stress on the semiconductor devices, and simplicity of design. These advantages are desirable features for high-power and high-voltage applications. The modelling and simulation result of Bridgeless Continuous Conduction Mode SEPIC Power Factor Correction rectifier is presented.

II. BRIDGELESS SEPIC PFC RECTIFIER

The bridgeless PFC circuits based on SEPIC with low conduction losses, is shown in Fig 2. Unlike the boost converter, the SEPIC converters offer several advantages in PFC applications, such as easy implementation of transformer isolation, inherent inrush current limitation during start-up and overload conditions, lower input current ripple.

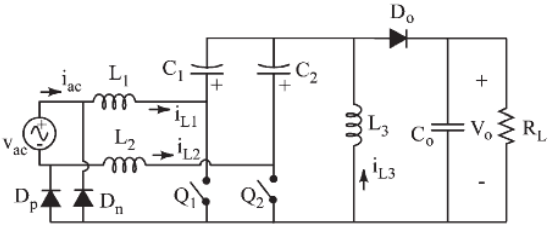

Fig 2: Bridgeless SEPIC PFC rectifier

The topologies in Figure 1are formed by connecting two DC–DC SEPIC Converter one for each half-line period of the input voltage The operational circuits during positive and negative half-line period for the proposed bridgeless SEPIC rectifier of Fig.2 is shown respectively. Note that, by referring to Fig.2 there are one or two semiconductors in the current flowing path. Each of the rectifiers utilizes two power switches (Q_1 and Q_2), two low-recovery diodes (Dp and Dn), and a fast diode (Do). However, the two power switches can be driven by the same control signal, which significantly simplifies the control circuitry. Moreover, the structure of the proposed topologies utilizes one additional inductor compared to the conventional topologies, which are often described as a disadvantage in terms of size and cost.

III. PRINCIPLE OF OPERATION OF THE BRIDGELESS RECTIFIER

The bridgeless rectifier shown in Figure 1 is constructed by connecting two DC–DC converters. Referring to Figure 3 during the positive half-line cycle, the first DC–DC SEPIC circuit L_1-Q_1-C_1-L_3-Do is active through diode Dp, which connects the input ac source to the output ground. During the negative half-line cycle, the second DC-DC SEPIC circuit, L_2-Q_2-C_2-L_3-Do, is active through diode Dn, which connects the input ac source to the output ground. Thus, due to the symmetry of the circuit, it is sufficient to analyze the circuit during the positive half-period of the input voltage. The rectifier is operated when the switch Q_1 is turned on then diode Dp is forward biased by the sum inductor currents i_{L1} and i_{L2}. As a result, diode Dn is reversed biased by the input voltage. The output diode is reversed biased by the reverse voltage (V_{ac}+ Vo). Thus, the loss due to the turn-on switching losses and the reverse recovery of the output diode are considerably reduced.

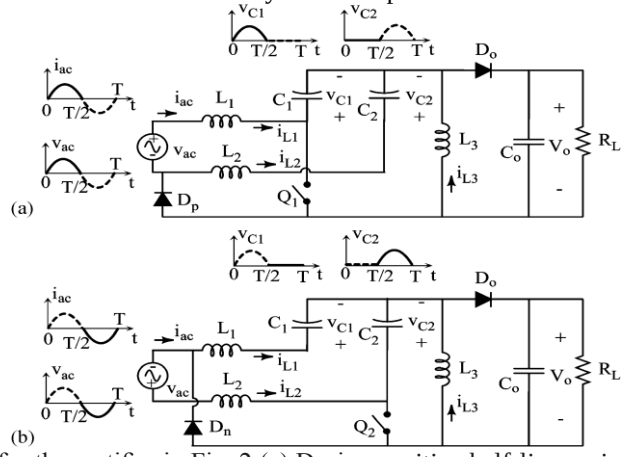

Fig. 3. Equivalent circuits for the rectifier in Fig. 2 (a) During positive half-line period. (b) During negative half-line period of the input voltage.

IV. COMPARISION BETWEEN CONVENTIONAL AND BRIDGELESS SEPIC PFC RECTIFIER

The circuit components in both the conventional PFC SEPIC rectifier and the improved bridgeless PFC SEPIC have similar peak voltage and current stresses. However, the bridgeless SEPIC is subjected to the input inductors (L_1 and L_2), the coupling capacitors (C_1 and C_2), and the active switches (Q_1 and Q_2) to a lower rms current stress compared to their counter parts in the conventional SEPIC topology. Moreover, the bridgeless SEPIC is constructed by connecting two DC–DC converters, each operating as SEPIC DC-DC converter, the switching performance of the two converters remains the same, which results in switching losses. Table 1 gives the comparison between conventional and bridgeless SEPIC PFC based on the equipments and current conduction path.

Table 1: Comparison Between Conventional And Bridgeless SEPIC PFC Rectifier

PFC Converter	Slow diode	Fast diode	Switch	Conduction path On/(Off)
Conventional SEPIC	4	1	1	2 slow diodes, 1 switch/(2 slow diodes,1 fast switch)
Bridgeless Sepic	2	1	2	1 slow diode, 1 switch/(1 slow diode ,1 fast diode)

V. SIMULATION RESULTS

The simulation result discussed by the Bridgeless SEPIC PFC rectifier is shown in Fig 4.

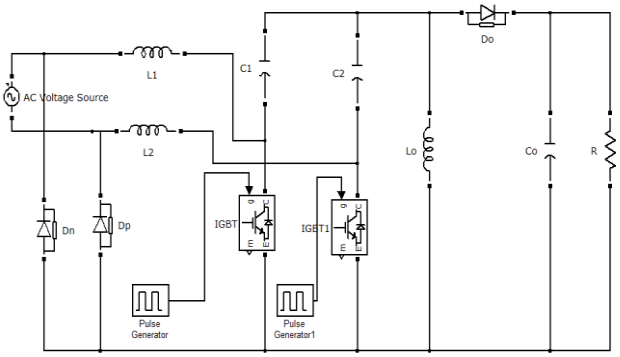

Fig 4: Simulation circuit of Bridgeless SEPIC PFC rectifier

For an input rms voltage of 100V, it produces an output DC voltage of 42V; the respective obtained results are displayed in Fig 6.

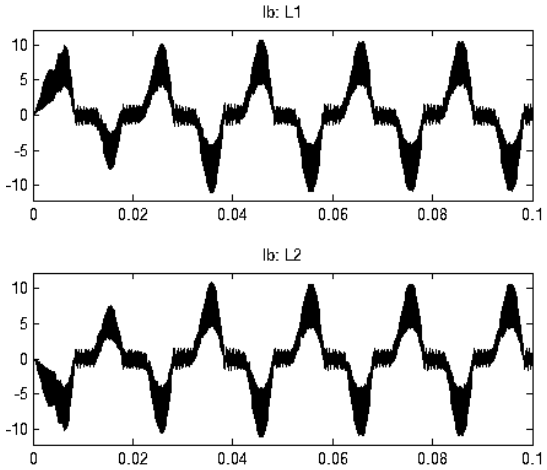

Fig 5: Current through inductor L_1 and L_2

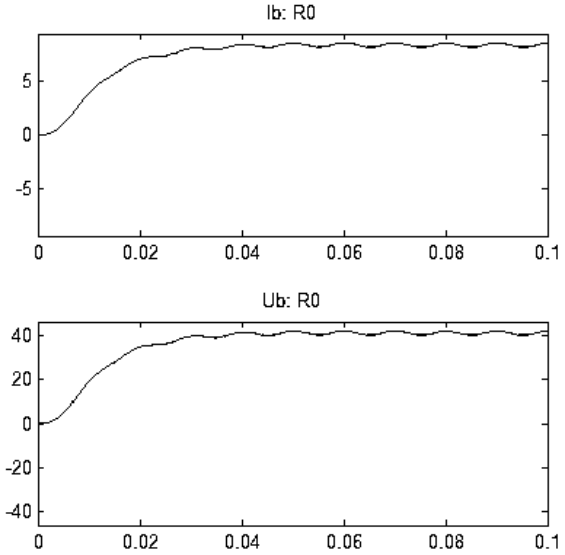

Fig 6: Output DC Current and DC voltage waveform

VII. CONCLUSION

The single-phase bridgeless rectifiers with low input current distortion and low conduction losses have been presented and analysed. The bridgeless rectifier is derived from the conventional SEPIC converter. Comparing with conventional SEPIC and Power Factor Correction circuits, due to the lower conduction loss and switching loss. Bridgeless SEPIC PFC rectifier topologies can further improve the conversion efficiency. To maintain same efficiency, the improved circuits could operate with higher switching frequency. Thus, additional reduction in the size of PFC inductor and EMI filter could be achieved. Besides improving circuit topology and performance, a further reduction in rectifier size could be realized by integrating the three inductors into a single magnetic core.

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