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DVR Using Diode Clamped Multilevel Inverter with Multicarrier Based Pulse Width Modulation Technique

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Abstract:- The Quality of the output power from the utilities has become a major concern of the modern industries. These power quality associated problems are voltage sag, surge, flicker, voltage imbalance, interruptions and harmonic problems. These power quality problems may cause problems to the industries ranging from malfunctioning of equipment to complete plant shut down. It has been identified that power quality can be degraded both due to utility side abnormalities as well as the customer side abnormalities. Voltage sag and swells in the medium and low voltage distribution grid are considered to be the most frequent type of power quality problems based on recent power quality studies. Their impact on sensitive loads is severe. Different solutions have been developed to protect sensitive loads against such disturbances but Dynamic Voltage Restorer (DVR) is considered to be the most efficient and effective solution. In this project, Dynamic Voltage Restorer (DVR) is implemented using fifteen level diode clamped multilevel inverter with Phase Opposition Disposition (POD) and Alternate phase opposition disposition pulse width modulation(APOD). In POD technique, four carrier waveforms are arranged so that all carrier waveforms above zero are in phase and they are 180 degrees out of phase with those below zero. In APOD technique, Carriers are arranged in such a manner that each carrier is out of phase with its neighbor by 180 degrees. The gate signals for the chosen inverter can be derived directly from the PWM signals .This is the difference between the POD and APOD multi carrier PWM technique. The main aim is to reduce the harmonic distortion and to mitigate the voltage sag. Thus the Power quality of the proposed system is expected to improve. Simulations are carried out using MATLAB/SIMULINK to verify the performance of the proposed method.

Keywords:- Dynamic Voltage Restorer (DVR), Phase Disposition PWM(PDPWM), Phase Opposition Disposition(PODPWM), Alternate Phase Opposition Disposition(APODPWM),Diode Clamped Multilevel Inverter (DCMLI).

I. INTRODUCTION

Power quality is certainly a major concern in the present era; it becomes especially important with the introduction of sophisticated devices, whose performance is very sensitive to the quality of power supply. Modern industrial processes are based on a large number of electronic devices such as programmable logic controllers and adjustable speed drives. The electronic devices are very sensitive to disturbances and thus industrial loads become less tolerant to power quality problems such as voltage dips, voltage swells, and harmonics.

Voltage sags can occur at any instant of time, with amplitudes ranging from 10-90% and a duration lasting for half a cycle to one minute. Voltage swell, on the other hand, is defined as an increase in rms voltage or current at the power frequency for durations from 0.5 cycle to 1 minute, typical magnitudes are between 1.1 and 1.8 pu. Voltage swells are not as important as voltage sags because they are less common in distribution systems. Voltage sags and swell can cause sensitive equipment to fail, or shutdown, as well as creates a large current unbalance that could blow fuses or trip breakers. These effects can be very expensive for the customer, ranging from minor quality variations to production downtime and equipment damage.

Series connected custom power devices are used to prevent sensitive load from sag interruption in the source side. Static Synchronous Series Compensator (SSSC) and Dynamic Voltage Restorer (DVR) both are presently used for series voltage sag compensation. Operating principle and functioning of these devices differ significantly as the SSSC injects a balance voltage in series whereas the DVR compensates the unbalance in supply voltage of different phases. The DVR supplies the active power with the help of DC energy storage and required reactive power is generated internally without any means of DC storage. The DVR can compensate voltage at both transmission and distribution sides [3]. Usually a DVR is installed on a critical load feeder. During the normal operating condition (without sag condition) DVR operates in a low loss standby mode. During this condition the DVR is said to be in steady state. When a disturbance occurs (abnormal condition) and supply voltage deviates from the nominal value, DVR supplies voltage for compensation of sag and is said to be in transient state [2].

II. DYNAMIC VOLTAGE RESTORER

The Dynamic Voltage Restorer (DVR) is fast, flexible and efficient solution to voltage sag problem [2]. It is a powerful electronic based device that provides three phase controllable voltage source, whose voltage vector (magnitude and angle) adds to the source voltage during sag event, to restore the load voltage to pre-sag conditions. It is designed for protecting the whole plant with loads in the range of some MVA. It can restore the load voltage within few milliseconds.

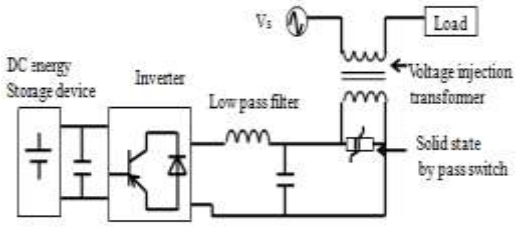

Fig.1 Schematic diagram of DVR

The Fig.1 represents the schematic diagram of DVR. It contains the basic configuration and components as follows:

DVR BASIC CONFIGURATION AND COMPONENTS

During voltage sags, the DVR injects a voltage to restore the load supply voltages. The DVR needs a source of this energy. Two types of system are considered, one using stored energy to supply the delivered power and the other having no internal energy storage, where energy is taken from the incoming supply through a shunt converter.

A. INVERTER CIRCUIT

The Voltage Source Inverter (VSI) or simply the inverter, converts the DC voltage of the energy storage unit (or the DC link) to a controllable three phase AC voltage [13]. The inverter switches are normally fired using a sinusoidal Pulse Width Modulation (PWM) scheme. Since the vast majority of voltage sags seen on utility systems are unbalanced, the VSI will often operate with unbalanced switching functions for the three phases, and must therefore treat each phase independently. Moreover, a sag on one phase may result in a swell on another phase, so the VSI must be capable of handling both sags and swells simultaneously [3]. Another topology of the DVR is the use of the multi - inverter system in the cascade. This method gets rid of the injection transformer used in the basic configuration of the DVR. This arrangement is often called a transformer-less or multilevel or a cascade inverter DVR.

B. FILTERING UNIT

The nonlinear characteristics of semiconductor devices cause distorted waveforms associated with high frequency harmonics at the inverter output. To overcome this problem and provide high quality energy supply, a harmonic filtering unit is used. These filters can be placed either in the inverter side or in the line side.

C. SERIES INJECTION TRANSFORMER

Three single-phase injection transformers are used to inject the missing voltage to the system at the load bars. To integrate the injection transformer correctly into the DVR, the MVA rating, the primary winding voltage and current ratings, the turn-ratio and the short-circuit impedance values of transformers are required. The existence of the transformers allow for the design of the DVR in a lower voltage level, depending upon the stepping up ratio.

III. MULTILEVEL INVERTERS

Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control [11]. The main concept of this inverter is to use diodes to limit the power devices voltage stress. A n level inverter needs (n-1) voltage sources, 2 (n-1) switching devices and (n-1) (n-2) diodes.This paper presents the most important topologies like diode-clamped inverter (neutral-point clamped) with separate DC sources [6]. The term multilevel starts with the three-level inverter. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion [1]. However, a high number of levels increases the control complexity and introduces voltage imbalance problems. [9]. In a five level diode clamped inverter consists of 8 switches, 12 diodes and 4 capacitors.

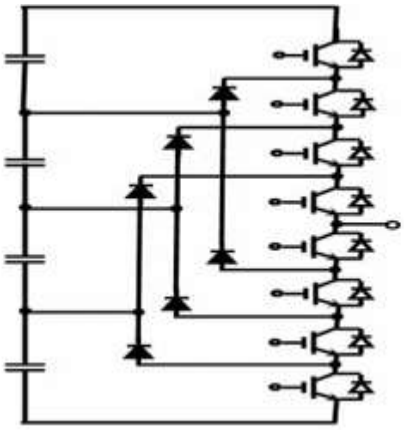

Fig.2 Five level diode clamped inverter

A 5-level diode clamped multilevel inverter is shown in Fig.2. For example to have Vdc/2 in the output, switches S1 to S4 should conduct at the same time. For each voltage level four switches should conduct. As it can be seen , the maximum output voltage at the output is half of the DC source [8]. It is a drawback of the diode clamped multilevel inverter. This problem can be solved by using a two times voltage source or cascading two diodes clamped multilevel inverters. We have seen DVR using diode clamped fifteen level multilevel inverter with phase disposition multicarrier PWM technique.

IV. CONTROL TECHNIQUE

A.PHASE DISPOSITION PWM (PDPWM)

The rules for phase disposition method for a multilevel inverter are four carrier waveforms in phase are arranged [12]. The converter is switched to + Vdc/2 when the sine wave is greater than both upper carrier. The converter is switched to + Vdc/4 when the sine wave is greater than the first upper carrier. The converter is switched to zero when a sine wave is lower than upper carrier but higher than the lower carrier. The converter is switched to – Vdc/4 when the sine wave is less than first lower carrier. The converter is switched to - Vdc/2 when the sine wave is less than both lower carriers. The following formula is applicable to sub harmonic PWM strategy i.e. PD, POD and APOD. The frequency modulation index

$$mf = fc/fm$$

The Amplitude modulation index

$$ma = 2Am/ (m-1) Ac$$

where fc – Frequency of the carrier signal
fm – Frequency of the reference signal
Am –Amplitude of the reference signal
Ac – Amplitude of the carrier signal
m- Number of levels.

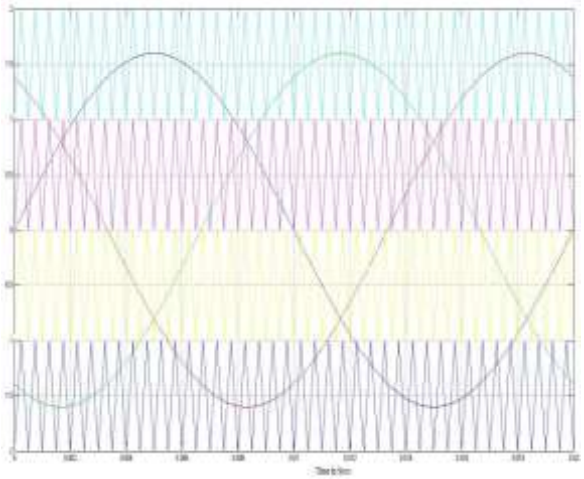

Fig. 3 Carrier arrangement for PDPWM strategy

Carrier arrangement for PDPWM strategy is shown in fig. 3. PDPWM technique consists all four carrier waveforms are in phase. In this technique the carrier amplitude is increased and compared to the original signal to generate the pulses. The voltage sags problem can be rectified by DVR with corresponding time period [7].

PROPOSED METHOD

B.PHASE OPPOSITION DISPOSITION (PODPWM)

Four carrier waveforms are arranged so that all carrier waveforms above zero are in phase and they are 180 degrees out of phase with those below zero.

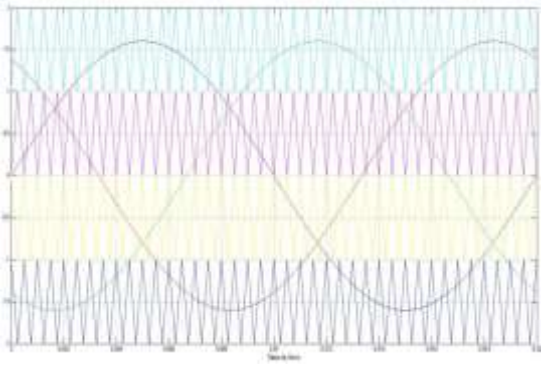

Fig.4 Carrier arrangement for PODPWM strategy

C.ALTERNATIVE PHASE OPPOSITION DISPOSITION (APODPWM)

Carriers are arranged in such a manner that each carrier is out of phase with its neighbor by 180 degrees.

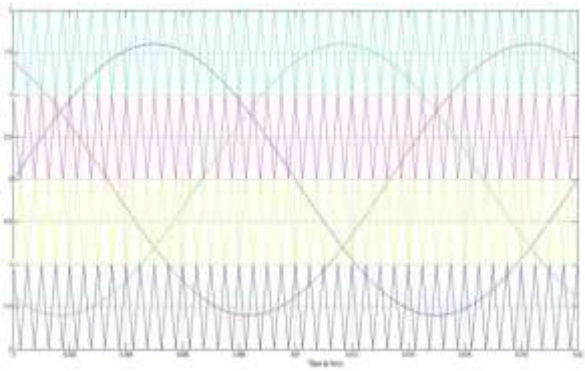

Fig.5 Carrier arrangement for APOD PWM strategy

V. DVR USING DIODE CLAMPED MULTILEVEL INVERTERS

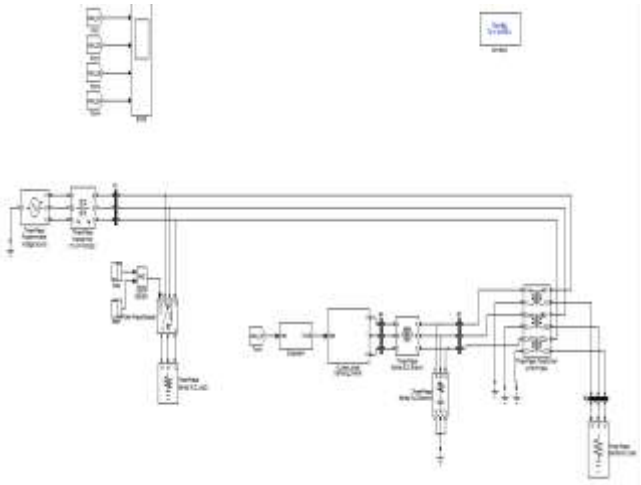

Fig .6 DVR using Diode Clamped Multilevel Inverters with PDPWM

DVR using the Diode Clamped Multilevel Inverter is shown in fig. 6. The main aim of this project is to mitigate the voltage sag and improves the power quality. One such reliable customer power device used to address the voltage sag, swell problem is the Dynamic Voltage Restorer [4]. In this circuit diagram, the three phase source supplies the source voltage (grid voltage) which can be measured by the voltage measurement block which is placed beside it. A breaker circuit which is placed in between the source and load induces the voltage sag. Two step signals are used to set the intermediate values at which voltage sag occurs. During that particular interval of time (to which the step signals are set) a pulse is given to breaker circuit which is initially at open condition. As soon as the pulse is received, the breaker circuit closes thereby allowing the supply of voltage to the heavy load to which it is connected. Thus the voltage supply to the load drops (decreases) at this particular interval .This voltage drop is known as voltage sag. The simulated result of the above schematic diagram is shown below, the intermediate values at which sag occurs is set from 0.1 Sec to 0.3 Sec. It contains B1 which is used to produce the input sag voltage. B2 represents the output area (compensate voltage). B3 denote the injected voltage. B4 represents the multilevel inverter part. After the sag produced, Vabc is the feedback input voltage given to the subsystem block. In this block the corresponding sine pulse is to be generated. Vabc is to be splitted into individuals Va, Vb, Vc subsystem, the carrier signal is to be produced. It contains the lookup table in which the carrier amplitude is to be increased the corresponding carrier pulse is to be generated. This is the concept of the phase disposition PWM and it is compared to the original signal [10]. Va, Vb, Vc are all combined to produce the corresponding gate pulse. That gate pulse is given the input of the diode clamped multilevel inverter. The corresponding output voltage is to be produced. Hence the load voltage is same as grid voltage without any power quality disturbances .I.e. The voltage sags/swell is compensated. Similarly the simulation are carried out by two control techniques namely PODPWM and APODPWM and the results are compared.

VI. SIMULATIONS AND RESULTS

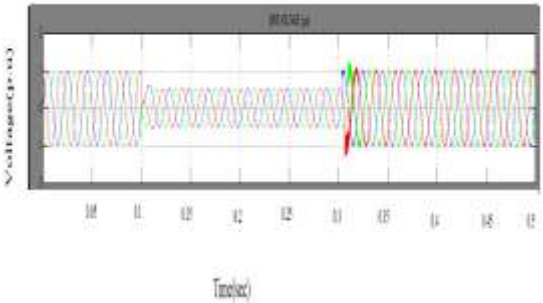

Fig.7 Waveform of grid voltage

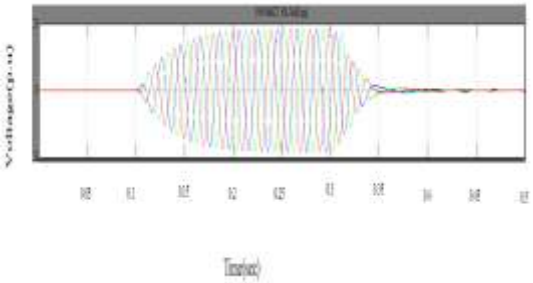

Fig .8 Waveforms of DVR injected voltage

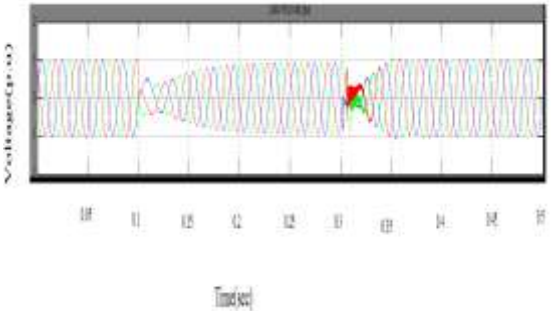

Fig .9 Waveforms of compensated load voltage

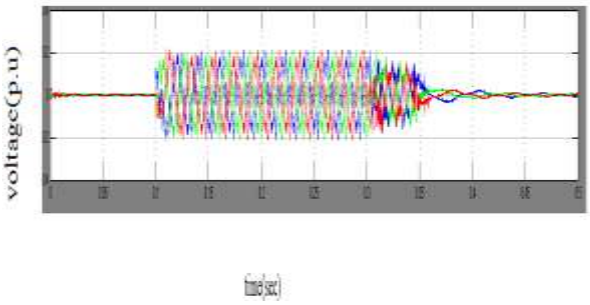

Fig.10 Output waveforms of fifteen level inverter

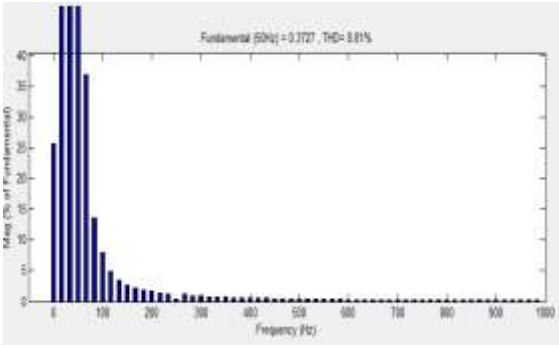

Fig.11 FFT Analysis of Phase Disposition PWM

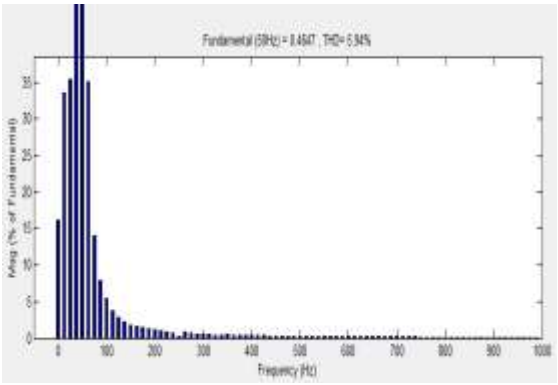

Fig.12 FFT Analysis of Phase Opposition PWM

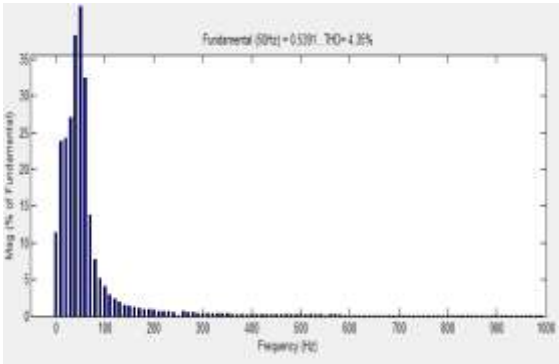

Fig.13 FFT Analysis of APOD PWM

In Fig. 7, it represents the waveform of grid voltage. The voltage sag occurs between 0.1 Sec to 0.3 Sec. After the DVR voltage is injected as shown in Fig.8. The main purpose is to compensate the voltage sag. In this technique phase disposition pulse width modulation is used to compare the original signal and the reference signal. The corresponding carrier pulse is generated. The waveform of compensated load voltage is as shown in Fig. 9. The main aim is to improve the power quality. The overall output waveform of diode clamped

multilevel inverter is shown in fig. 10. Similarly the results are compared with PODPWM and APODPWM techniques.

Comparison Results:

Factor	PDPWM	PODPWM	APODPWM
THD%	8.81	5.50	4.35

VII. CONCLUSION

In this paper, the implementation of DVR using diode clamped multilevel inverter with phase disposition pulse width modulation. Voltage sags problem can be rectified by Dynamic Voltage Restorer. The main function of the DVR is to monitor the load voltage waveform constantly and if any sag or surge occurs, the balance voltage is injected to the load voltage. The PD PWM technique is used, the carrier amplitude is increased and compared to the original signal to generate the carrier pulse. The main aim is to improve the power quality and to compensate the voltage sag.

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