Study of Soft-Switched Isolated DC-DC Converters for Auxiliary Railway Supply Using DC Machine

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Abstract:- In modern railways coaches, the electrical separation between the high voltage side and the auxiliary equipments on the consumer side is realized by means of heavy and bulky 50-Hz Transformers. In order to reduce the weight and size of the devices, today new power supply systems are proposed that consist in soft-switched isolated dc-dc converters with a lightweight medium frequency transformer and diverse output modules supplied by a common 600-V dc intermediate circuit. This paper aims to investigate in detail two such solutions of isolated dc-dc converters for auxiliary railway supply where zero-current transitions are achieved for the primary inverter switches.

Index Terms:- Auxiliary over supply ,dc-dc converters railway traction , soft switching

I. INTRODUCTION

Railway power supply system's need to be expanded and operated more efficiently due to increased transport demands on rail and increased energy economy awareness. Generally speaking, an electric railway power supply system (RPSS) differs from a public transmission or distribution system in many ways. Briefly, the loads of RPSSs, i.e. the trains, are moving, and the size of the loads varies with time and location. Power consumption increases with speed, weight, acceleration, inclination (gradients) and horizontal curvature, etc. Trains can also regenerate, when braking electrically, and then the RPSS also has moving distributed generation sources. Moreover, it is not uncommon that the loads of the trains are so high that voltage drops in the contact line system are much larger than what is allowed in public power grids. New power supply systems are considered that consist of soft-switched dc-dc converters and diverse output modules supplied by a common 600-V dc intermediate circuit. The input and output sides are electrically separated by a lightweight medium frequency (MF) transformer (typically several kilohertz). Such an approach is in keeping with other research activities that have been going on in railway traction to substitute the low frequency transformer, commonly used to reduce the line voltage to a level more convenient for motors, by alternative solutions, either with an intermediate conversion stage using MF transformers ("MF topologies") or by means of transformer less configurations.

To enable operating at high frequency with reduced EMI and switching losses, several soft-switching techniques for high-power isolated dc-dc converters have been proposed in the literature. These can be classified into two groups, namely zero-voltage switching (ZVS) and zero-current-switching (ZCS), where the soft transitions are (most often) achieved by the use of an auxiliary circuit that creates some form of inductance– capacitance (*LC*) resonance. The present contribution aims to investigate two different solutions of half bridge zero-current switching pulse-width modulation (HB-ZCS-PWM) dc-dc converters for auxiliary railway supply. It follows previous works devoted to ZVS isolated dc-dc converters for railway applications.

The first converter topology, suggested by Al storm Transport, makes use of an auxiliary circuit somewhat similar to that considered in, which is attached to the secondary side of the MF transformer in order to achieve ZCS. The proposed solutions, using 6.5-kV IGBT transistors as high-voltage switches , should meet the requirements of operating conditions listed in Table I, where the main working parameters are the input voltage, subject to wide variations, and the output current that can vary from no load up to twice the value of the rated current (at 3-kV nominal input).

II. PROPOSED TOPOLOGY

The first HB-ZCS-PWM dc-dc converter topology is shown in Fig. 3. A simple auxiliary circuit consisting of a resonant capacitor C_a and an auxiliary switch S_a is attached to the secondary side in order to achieve ZCS for the primary switches S_+ and $S_- .L_k$ refers to the leakage inductance of the transformer. $D_1 \sim D_4$ are the output rectifier diodes. , V_d , V_0 , and I_0 are the dc input voltage, output voltage and output current, respectively. The transformer turns ratio is denoted by m (primary to secondary). Fig. 5 shows the operational

key waveforms of the converter. One cycle period $T_s = \frac{2\pi}{\omega_s}$ is divided into two half cycles, $t_0 \sim t_5$ and $t_5 \sim t_{10}$ because the operating principles of two half cycles are symmetric, only the first half cycle is explained. This half-cycle is divided into five modes. For convenience of the mode analysis in the steady state, several assumptions are made as follows. All components used in this converter have ideal characteristics; the transformer leakage inductance will, however, not be neglected C_+ , C_- and L_0 are large enough to be considered as constant voltage sources $V_d/2$, $V_d/2$, and constant current source I_0 respectively. Each operating mode is simply described as follows.

Mode $1[t_0 \sim t1]$: In this mode, S. turns on and the power is delivered from the input to the output. This operating mode is just the same as for a conventional hard switching PWM HB converter.

Mode $2[t_1 \sim t_2]$: At time, the auxiliary switch S_a turns on, the resonance between L_k and C_a starts. At ,t₂ the Voltage across the resonant capacitor reaches $m \cdot V_d$ and the transformer secondary side current decreases to the value Of the output current I_0 . Referring to Fig. 4, the resonant voltage across Ca and the resonant current in Lk are given

$$V_{c} = \frac{mV_{d}}{2} [1 - \cos(\omega_{0}(t - t_{1}))]$$
(1)

$$I_{2} I_{0} + \frac{mV_{d}}{2\pi_{0}} \sin(\omega_{0}(t - t_{1}))$$
(2)

Where
$$\omega_0 = 1/\sqrt{(L_K \cdot C_a)}$$
 and $Z_0 = \sqrt{(L_K \cdot C_a)}$

Mode $3[t_2 \sim t_3]$: At time t_2 , the capacitor current reverses and now must flow through the antiparallel diode of S_a . In the same time, S_a can be turned off with ZCS. The resonant capacitor is discharged according to (1) and the secondary current decreases to zero according to (2).

Mode $4[t_3 \sim t4]$: At time t_3 , the secondary current reduces to zero and cannot change direction. The reflected current in the primary side is cancelled in S_a. The switch can therefore be turned off with ZCS at t_3 . During this mode, the output rectifier diodes are all turned off, while the resonant capacitor C_a is discharged linearly by the output current I0_a

Mode 5 $[t_4 \sim t5]$: At t₄, the voltage across C_a reduces to Zero and the capacitor current is forced to zero (it corresponds to area in A=B Fig. 5). The output current I₀ Freewheels through D1~D₄ and the secondary voltage Reduces to zero. Since S₊ and S₋ are both turned off, the Primary current cannot flow and the primary voltage is imposed to zero by the secondary. From the previous analysis, the first topology of dc-dc converter achieves ZCS for both the primary and auxiliary switches. The operating modes during the subsequent half cycle are symmetric to those described previously. It should be noticed that the anti-parallel diodes of the primary switches (commercial IGBT modules) are not used during operation. Hereafter, the equations will be normalized by using the base voltage and current

$$V_{\text{base}} = \mathbf{m} \cdot \mathbf{V}_{\text{d}}/2 \tag{3}$$

$$I_{\text{base}} = V_{\text{base}}/Z_0 \tag{4}$$

Assuming that the resonant capacitor is completely discharged at , $t_0 + T_s/2~$ the steady-state output voltage characteristics for different values of $D_{aux}~$ and a given applied input voltage $~V_d~$ can be expressed as follows:

$$V_{0N} = 2D_{aux} + \frac{\kappa}{\pi} [(\boldsymbol{\alpha} + \pi) + I_{0N} + \frac{1}{2I_{0N}} (\cos \boldsymbol{\alpha} + 1)^2]$$
(5)

Where the ratio $\omega_s\!/\,\omega_0\,$ is simply denoted by K , the operational duty cycle $D_{aux}\,$ is defined from the time delay between t_0 and the turn-on of $\,S_a$, and

$$\alpha = \arcsin(I_{oN})$$

Note that the normalized quantities are denoted by an additional subscript "N." For given values of the applied input voltage and the operational duty cycle D_{aux} , the minimum load current can be determined in solving the following implicit expression:

$$I_{0,\min} = \frac{1 + \cos\alpha_{\min}}{\frac{\pi}{K} \cdot (1 - 2D_{aux}) - (\alpha_{\min} + \pi)}$$
(7)

Which expresses the voltage across Ca exactly reduces to zero at the end of a half-cycle, i.e., at $t_4=t_5(=t_0+T_s/2)$



Fig 1 Proposed topology of HB-ZCS-PWM dc-dc converter.



III. PRINCIPLE OF OPERATION

Resonant Components: In order to achieve ZCS for the primary switches in every load conditions, the peak resonant current in the auxiliary circuit should be larger than the maximum output current. Therefore, according to (2), and should satisfy

$$\sqrt{\frac{L_k}{C_a}} \le \frac{1}{2} \frac{m v_d}{I_{0,max}} \tag{11}$$

Where I0max is the maximum output current. Otherwise stated, for given transformer characteristics m and L_k , the following

$$C_a \ge C_{a,min}$$
 (12)
Where

$$C_{a,\min} = 4L_k \cdot \left(\frac{l_{0,max}}{mV_d}\right)^2$$
(13)

The resonant period of L_k and Ca should be limited to a reasonable part of the whole switching period. In practice, the minimum turn on time of the primary switches S_+ and S_- should be larger than the required turn on time of the auxiliary switch, which is determined by the resonant period. If the resonant period is too long, the required minimum duty cycle D will be increased. Otherwise, the ZCS condition will be lost at some particular conditions. Usually, the resonant period should therefore be a small part of the switching period, which can be expressed as

$$T_0 = 2\pi \cdot \sqrt{L_k C_a} = K \cdot T_s \tag{14}$$

Where T0 (= $2\pi/\omega_0$) is the resonant period, T_s the switching period, and represents the maximum acceptable value of T_0/T_s

This should be limited to a reasonable value (say 20%). Based on (12)–(14), the resonant parameters can be calculated

And the smaller one should be adopted in the design.

2) Power Devices: The design equations reported in Table I provide suitable ratings of the power semiconductor devices under worst case operating conditions to ensure proper operation of the converter. For reasons of conciseness, the complete Developments of the proposed design equations cannot be exposed here. Still these have been derived by applying the conventional definitions of the peak, average, and rms values to the devices voltage and current idealized waveforms (deduced from the previous theoretical analysis in Section II). Using (5) (non-normalized), the auxiliary duty cycle was also substituted with an expression in terms the output voltage and the output current. The ratings of the devices calculated from the given design equations provide a good approximation for the final values used in an actual implementation which, however, may be somewhat different due to other practical considerations .The maximum and minimum peak resonant current through the resonant capacitor C_a are defined by

$$I_{c,max} = \frac{m \cdot V_{d,max}}{2Z_0}$$
$$I_{c,min} = \frac{m \cdot V_{d,min}}{2Z_0} (15)$$

Referring to Table II, the maximum voltage stress across both the primary and secondary power devices occurs at the Maximum input voltage $V_{d,max}$. Under the condition that the output voltage is properly regulated, the maximum current Stress through the sec ondary side devices arises for the maximum output current and the maximum input voltage (i.e., for The highest value of the peak resonant current). In the primary side, it is noticed that the maximum stress in terms of average And rms currents through the primary switches, S_+ and S_- , occurs at the minimum input voltage. Note that, in order to calculate the rms currents reported in Table II, we also defined

$$\boldsymbol{\alpha}_{1} = \arcsin(\frac{l_{0,max}}{l_{C,min}}) , \boldsymbol{\alpha}_{2} = \arcsin(\frac{l_{0,max}}{l_{C,max}})$$
(16)
hence, $\boldsymbol{\xi}_{1} = \cos(\boldsymbol{\alpha}_{1})$ and $\boldsymbol{\xi}_{2} = \cos(\boldsymbol{\alpha}_{2})$.

Table I ANALYTICAL EXPRESSIONS OF THE MAXIMUM VOLTAGE AND CURRENT STRESSES OF THE POWER DEVICES USED IN TOPOLOGY

Power	Peak	Peak ,average and rms currents
devic	voltage	
es		
S_+ , S	$V_{S,peak} = V$	$\mathbf{I}_{\mathrm{S,peak}} = \mathbf{m} \cdot (\mathbf{I}_{0,\max} + \mathbf{I}_{\mathrm{c,max}}), \mathbf{I}_{\mathrm{S,ave}} = \frac{V_0 \cdot I_{0,max}}{V_d \cdot min},$
	d,max	$I_{S,rms} = m \cdot \sqrt{\frac{V_0 \cdot I_{0,max}^2}{m \cdot V_{d,min}} + \frac{K}{2\pi} \left(-\frac{I_{0,max}^3}{I_{C,min}} + (-\xi_1^2 + \xi_1 + 3) \cdot \frac{I_{0,max} \cdot I_{C,min}}{2} + \frac{\alpha_1 + \pi}{2} \cdot I_{C,min}^2 \right)}$
Sa	V _{Sa}	$I_{\text{sa,peak}} = I_{\text{C,max}}, I_{\text{Sa,ave}} = \frac{2K}{L} \cdot I_{\text{C,max}}, I_{\text{Sa,rms}} = \frac{\sqrt{K}}{2} \cdot I_{\text{C,max}}$
	$\frac{peak}{mV_{d,max}}$	π σ , π
D _a	$V_{\text{Da,peak}} = \frac{mV_{d,max}}{2}$	$I_{\text{Da,peak}} = I_{\text{o,max}}, I_{\text{Da,ave}} = I_{\text{Sa,ave}}, I_{\text{Da,rms}} = \sqrt{\frac{K}{2\pi} \cdot \left((\xi_2 + 2) \cdot I_{0,max} \cdot I_{C,max} + \alpha_2 \cdot I_{C,max}^2 \right)}$
D ₁ ~	V _{D,peak}	$I_{D,peak} = \frac{IS, peak}{I_{D,peak}}, I_{D,peak} = \frac{I_{0,max}}{I_{D,peak}},$
D_4	$_{=}mV_{d,max}$	$\frac{D_{\mu\nu}}{m} = \frac{1}{2}$
		$\sqrt{(V_0 - 1) l_0^2 max} = k \left(\frac{l_0^3 max}{10} + \frac{1}{10} max} \right) = 2 - 2 - 2 - 2 - 2 - 2 - 2 - 2 - 2 - 2$
		$\sqrt{\left(\frac{1}{m \cdot V_{d,max}} + \frac{1}{2}\right)^{\frac{1}{2},max}} + \frac{1}{2} + \frac{1}{4\pi} \left(-\frac{1}{I_{C,max}} + (\alpha_2 + \pi) \cdot \left(2I_{0,max}^2 + I_{C,max}^2\right) - 3 \cdot \xi_2 \cdot (\xi_2 \cdot + 1)\right)$



Fig2. Matlab/Simulink Model of proposed Comparative Study of Soft-Switched Isolated DC-DCConverters for Auxiliary Railway Supply





Fig 6 waveforms of voltage and current across transformer



Fig 7 output of pulse generator

V. CONCLUSION

This paper has investigated topology of soft-switched isolated dc-dc converters for auxiliary railway supply. First, the operating principles and the design considerations have been presented in detail. Then, computer simulations have been conducted in accordance with the requirements of the specific railway application in order to verify the theoretical analysis. The steady-state output voltage characteristics at 3-kV input have been discussed for the topology, As an important requirement, the ability to supply 600-V output at light loads has also been studied from these characteristics ,here dc machine is used in place of resistive load then the output voltage is above 600v, Finally, a analysis of the topology has been carried out, the main outcomes are as follows: 1) the overall weight and size reduction of the passive components is rather in favour 2) even though less material is expected for as regards the transformer; 3) at rated conditions, the total power loss of the power semiconductor devices is significantly less for topology #1 (no hard-switching); 4) if the values of the resonant elements are changed within a prescribed tolerance, the two converters are still able to achieve ZCS;

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